(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 355 693 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89115107.8

(22) Date of filing: 16.08.89

(51) Int. Cl.4: G09G 3/36 , G02F 1/133

(30) Priority: 17.08.88 JP 205067/88
07.10.88 JP 254248/88

(43) Date of publication of application:
28.02.90 Bulletin 90/09

(84) Designated Contracting States:
AT BE CH DE ES FR GB GR IT LI LU NL SE

(71) Applicant: CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko
Ohta-ku Tokyo(JP)

(72) Inventor: Tsuboyama, Akira
2-28-10-203 Sagamidai
Sagamihara-shi Kanagawa-ken(JP)
Inventor: Ooki, Akiko
2-10-1 Asahicho
Atsugi-shi Kanagawa-ken(JP)
Inventor: Inoue, Hiroshi
1200-6-f-409 Kamariyacho Kanazawa-ku
Yokohama-shi Kanagawa-ken(JP)

(74) Representative: Grupe, Peter, Dipl.-Ing. et al
Patentanwaltsbüro
Tiedtke-Bühling-Kinne-Grupe-Pellmann-Grams-Struif-Winter-Roth Bavariaring 4
D-8000 München 2(DE)

(54) Display apparatus.

(57) A display apparatus includes: (a) a liquid crystal device comprising scanning electrodes, data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes, the scanning electrodes and data electrodes being disposed to intersect each other so as to form an electrode matrix and provide a display surface covering the electrode matrix, (b) first means for applying a scanning selection signal to the scanning electrodes and applying data signals to the data electrodes in synchronism with the scanning selection signal, and (c) second means for dividing the display surface into an effective display region and a non-display region and controlling the first means so as to apply a scanning selection signal to a scanning electrode covered by the non-display region in a shorter cycle than the application of a scanning selection signal to scanning electrodes covered by the effective display region.

EP 0 355 693 A2

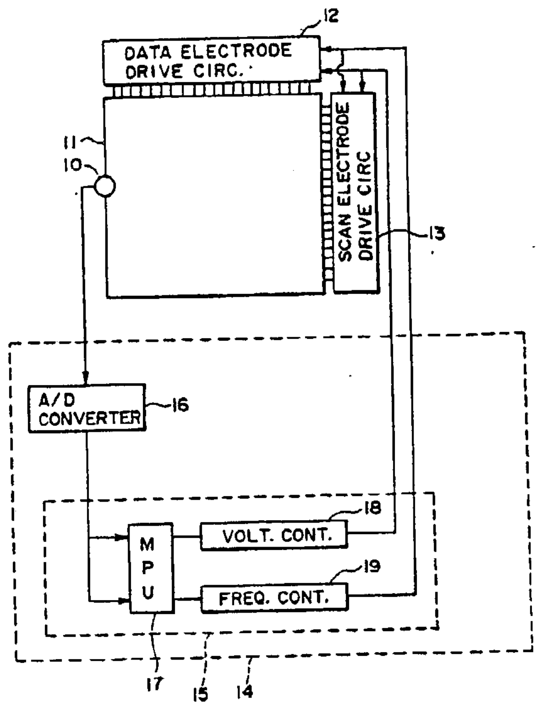

12
DATA ELECTRODE
DRIVE CIRC.
11
10
SCAN ELECTRODE
DRIVE CIRC
13
A/D
CONVERTER
16
18
M
P
U
VOLT. CONT.
19
FREQ. CONT.
17
15
14

FIG. 1

DISPLAY APPARATUS

FIELD OF THE INVENTION AND RELATED ART

The present invention relates to a liquid crystal apparatus, particularly a display apparatus using a ferroelectric liquid crystal.

Clark and Lagerwall have disclosed a surface-stabilized bistable ferroelectric liquid crystal in Applied Physics Letters, Vol. 36, No. 11 (June 1, 1980), pp. 899 - 901, and U.S. Patents Nos. 4,367,924 and 4,563,059. The bistable ferroelectric liquid crystal has been realized by disposing a chiral smectic liquid crystal between a pair of substrates which are set to provide a spacing small enough to suppress the formation of a helical arrangement of liquid crystal molecules inherent to the bulk chiral smectic phase of the liquid crystal and aligning vertical molecular layers each composed of a plurality of liquid crystal molecules in one direction.

A liquid crystal apparatus comprising such a ferroelectric liquid crystal may be driven by a multiplexing drive scheme as disclosed by, e.g., U.S. Patent No. 4,655,561 to Kanbe, et al., to provide a display with a large number of pixels.

Such a liquid crystal apparatus may be used as a display panel for a word processor, a personal computer, etc. In order to incorporate such a liquid crystal panel in a display apparatus, it is necessary to provide a housing framing the periphery of the panel. On the other hand, a liquid crystal panel has a cell structure comprising a pair of glass plates and a (ferroelectric) liquid crystal sandwiched therebetween, and it cannot generally provide a curved display surface like a CRT, so that the peripheral frame part of the housing masks a part of the display picture to an operator.

For the above reason, it has been necessary to define a part of the display surface which can be masked by the peripheral panel as a marginal non-display region and define the remaining part of the display surface which cannot be masked by the peripheral frame as an effective display region, so that the non-display region is always held in a white (or black) state and a display image is formed only on the effective display region by controlling a drive circuit.

There has been however observed a problem that if the display state of the non-display region is left to depend on the initial alignment of a ferroelectric liquid crystal, domains in a bright state and domains in a white state are co-present to result in a lower display quality.

Further, according to our experiments, in a higher region and a lower region than the effective display region of the non-display region masked by the peripheral frame, i.e., regions of the non-display region which are parallel with scanning electrodes in the effective display region and disposed outside the effective display region, it has been observed that the optical transmission state of white (or black) is fluctuated for respective scanning periods and that this is particularly pronounced at lower environmental temperatures where one scanning selection period is required to be longer to result in a lower frequency of scanning operation (frame or field operation), so that the fluctuation is recognized as flickering.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a display apparatus having solved the above-mentioned problem, particularly suppressing the flickering due to fluctuation in optical transmission state of white (or black) in a non-display region, to provide an improved display quality.

According to the present invention, there is provided a display apparatus, comprising:

(a) a liquid crystal device comprising scanning electrodes, data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes, the scanning electrodes and data electrodes being disposed to intersect each other so as to form an electrode matrix and provide a display surface covering the electrode matrix,

(b) first means for applying a scanning selection signal to the scanning electrodes and applying data signals to the data electrodes in synchronism with the scanning selection signal, and

(c) second means for dividing the display surface into an effective display region and a non-display region and controlling the first means so as to apply a scanning selection signal to a scanning electrode covered by the non-display region in a shorter cycle than the application of a scanning selection signal to scanning electrodes covered by the effective display region.

In a preferred embodiment, the above-mentioned second means comprises a means for dividing the display surface into an effective display region covering a total of M scanning electrodes and a non-display

region covering a scanning electrode and controlling the first means so as to apply a scanning selection signal to the scanning electrodes in the display region in such a manner that a scanning selection signal is applied to the scanning electrodes N electrodes apart (N: an integer of 1 or more) in one scanning operation and applied to all the M scanning electrodes covered by the display region in N+1 times of scanning operation, and to apply a scanning selection signal to the scanning electrode covered by the non-display region in a cycle during which the scanning selection signal is applied to M or less scanning electrodes, preferably M/(N+1) or less scanning electrodes, further preferably M/2(N+1) or less scanning electrodes, in the display region.

According to another aspect of the present invention, there is provided a display apparatus comprising a display apparatus, comprising:

(a) a display panel comprising scanning electrodes and data electrodes disposed to intersect the scanning electrodes so as to form a pixel at each intersection, and including a display region comprising a plurality of the pixels arranged in a plurality of rows and a plurality of columns and a marginal non-display region disposed outside the display region and constituted by a third electrode which is disposed in parallel with the scanning electrodes,

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an apparatus according to the present invention.

Figure 2 is a schematic plan view of a display apparatus.

Figure 3 is a plan view of a matrix electrode structure with drive circuits.

Figure 4 is a waveform diagram showing a set of driving signals used in the present invention.

Figures 5 and 6 are respectively a time-serial waveform showing a set of scanning signal voltages used in the present invention.

Figure 7 is a block diagram of another embodiment of the apparatus according to the present invention.

Figure 8 is an exploded perspective view of a display panel used in the present invention.

Figure 9 is a schematic sectional view of a display panel used in the invention.

Figure 10 is a block diagram of a control unit used in the invention.

Figure 11 is a block diagram of a data output unit used in the invention.

Figure 12 is a flow chart showing a display control sequence used in the invention.

Figure 13 is an explanatory diagram for illustrating an optimum drive characteristic.

Figures 14A - 14B and 15A - 15C are respectively a set of drive waveform diagrams used in the present invention.

Figure 15D is an example of a display state shown on an electrode matrix.

Figures 16 and 17 are schematic perspective views for illustrating ferroelectric liquid crystal cells used in the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 is a block diagram of a liquid crystal apparatus according to the present invention. Referring to Figure 1, the liquid crystal apparatus comprises a ferroelectric liquid crystal panel 11 which in turn comprises a matrix electrode structure composed of scanning electrodes and data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes (detailed structure not shown), a data electrode drive circuit 12, and a scanning electrode drive circuit 13. The liquid crystal apparatus is further equipped with a temperature sensor 10 (of, e.g., a thermistor) for detecting an environmental temperature and outputting a voltage within a prescribed range (e.g., 2.5 V - 0 V for a temperature range of 0 °C - 60 °C). The voltage value outputted from the temperature sensor 10 is subjected to digital conversion into a corresponding number of bits by an A/D converter 16 in a liquid crystal panel control circuit 14, and the number of bits is read and judged by an MPU (micro-processor unit) 17 in a drive waveform generation control unit 15. The resultant signal from the MPU 17 may be supplied to a voltage controller 18 and a frequency controller 19 to control output waveforms (one scanning selection period and drive voltage peak values) from the scanning electrode drive circuit 13 and the data electrode drive circuit 12.

Figure 2 is a plan view showing a display unit comprising a liquid crystal panel fixed with a peripheral frame 21 covering or masking the periphery of the liquid crystal panel. The display surface of the display panel is divided into an effective display region 22 and a non-display region 23 as described above.

Figure 3 is a plan view showing an electrode matrix constituting a display surface together with control circuits therefor. The electrode matrix comprises scanning electrodes including scanning electrodes 31 in the non-display regions 23 and scanning electrodes 32 in the effective display region 22 and data electrodes 33 intersecting with the scanning electrodes so as to form a pixel at each intersection. The scanning electrodes 31 and 32 are connected to the scanning electrode drive circuit 13 and the data electrodes 33 are connected to the data electrode drive circuit 12. In a preferred embodiment of the present invention, the scanning electrodes 31 in the non-display region 23 may be made broader than the scanning electrodes 32 in the effective display region 22 and may generally be formed in a width of about 1 mm - 10 mm. Further, in case of equal width, the scanning electrodes may be disposed in a plurality in each non-display region 23.

Figure 4 shows a set of drive voltage signal waveforms. In one scanning selection period, a scanning selection signal comprising alternating voltages V_1 and $-V_2$ and a voltage of 0 (the voltages V_1, $-V_2$ and 0 being values defined with respect to a scanning nonselection signal as the reference level). Each data electrode is supplied with a black (B) or white (W) data signal depending on given data concerning a desired optical state. In this particular embodiment, the pixels on a scanning electrode supplied with a scanning selection signal are simultaneously erased into a black state in a period T_1 during one scanning selection period, and in a subsequent period T_2, a pixel supplied with a data signal (B) is set to a black state and a pixel supplied with a data signal (W) is set to a white state.

Figure 5 is a waveform diagram showing an example of sequence of applying a scanning selection signal to the scanning electrodes. According to the scanning sequence shown in Figure 5, a scanning selection signal is sequentially applied to the scanning electrodes S_1, S_2, ..., $S_{F8+8(s-1)}$ every 8th electrode (7 electrodes apart) in one vertical scanning (field scanning) and one picture is formed through 8 times of field scanning to complete one frame scanning. In this instance, in each field scanning, the scanning selection signal is also applied to the scanning electrodes S_A and S_B in the non-display region. In Figure 5, the symbols F_1, F_2, ..., F_8 each represent an ordinal number of field scanning in one frame scanning and the symbol s represents an ordinal number of scanning in one field scanning.

In a preferred embodiment of the present invention, a scanning selection signal may be applied to the scanning electrodes S_A and S_B in the non-display region two or more times in each field scanning. For example, it is possible to apply a scanning selection signal to the scanning electrodes S_A and S_B at the time when a half of each field scanning is completed and also at the time when the remaining half of each field scanning is completed.

In the driving embodiment shown in Figure 5, in synchronism with the application of a scanning selection signal to the scanning electrodes S_A and S_B in the non-display region, only either one of the data signals (B) and (W) shown in Figure 4 is applied to the data electrodes 33 by controlling the data electrode drive circuit 12. Further, in synchronism with the application of a scanning selection signal to the scanning electrodes S_1, S_2, ..., $S_{F8+8(S-1)}$, data signals are selectively applied to the data electrodes corresponding to given data for a desired display.

We made a series of experiments wherein the above-mentioned display operation was repeated by using a ferroelectric liquid crystal panel with the dimensions and drive conditions as shown below and the driving signal waveforms shown in Figure 4 while applying the scanning selection signal to the scanning electrodes in the effective display region N electrodes apart (in every (N+1)-th electrode) with different number of N and effecting the above-mentioned drive to the scanning electrodes in the non-display region (i.e., as time-serially shown in Figure 5 with different numbers of skipped scanning electrodes).

<u>Ferroelectric liquid crystal panel</u>

Number of total scanning electrodes: 400
Scanning electrodes in the effective display region: 398
Width of each scanning electrode: 0.3 mm
Scanning electrodes in the non-display region: 2
With of each scanning electrode: 5 mm
Number of data electrodes: 640
Ferroelectric liquid crystal: "CS-1017" (trade name available from Chisso K.K.)
Peak values of drive signals,

V_1 = 15 volts
$-V_2$ = -15 volts
$\pm V_3$ = ±5 volts
One scanning selection period: 400 µsec
Temperature: 15 °C

The display states (flickering) on the panel were evaluated by a panel comprising arbitrarily selected 20 panelists (operators). The results are summarized in the following Table 1 wherein x denotes a case where 20 - 15 panelists recognized flickering in the non-display region; Δ , 14 - 6 panelists recognized flickering in the non-display region; and o, 20 - 15 panelists recognized no flickering in the non-display region.

Table 1

N (scanning N lines apart)	0	1	2	3	4	5	6	7	8
Spatial frequency (Hz)	6.3	12.6	18.9	25.2	31.5	37.8	44.1	50.4	56.9
Evaluation of flickering	x	x	Δ	o	o	o	o	o	o

From the above results, it has been found that a display substantially free from flickering in the non-display region could be realized in the cases where the scanning was effected N or more scanning electrodes apart and the scanning electrodes in the non-display region were driven in each field scanning. Further, in the case of the scanning 2 electrodes apart, no flickering was recognized either when the scanning electrodes in the non-display region were driven in each half field scanning.

The above driving experiment was repeated by using the scanning signal waveforms time-serially shown in Figure 6 instead of those shown in Figure 5 with varying numbers of skipped scanning electrodes, whereby similar results as in the above embodiment were obtained. In the driving embodiment shown in Figure 6, the scanning electrodes S_A and S_B in the non-display region were supplied with a non-display voltage signal pulse for providing the pixels on the scanning electrodes S_A and S_B simultaneously with a white (or black) state regardless of the kinds of display signals applied thereto. More specifically, the non-display voltage signal pulse in the experiment had a peak value ($-V_4$) to -20 volts and a duration of 400 µsec which was the same as one scanning selection period used for writing in the effective display region.

Figure 7 is a block diagram of another embodiment of the display apparatus according to the present invention. The display apparatus includes a display panel 100 comprising an FLC (ferroelectric liquid crystal), a word processor main frame 71 as a host apparatus functioning as a source of supplying display image data to the display panel 100, and a display control apparatus 50 for controlling the drive of the display panel 100 depending on the display data supplied from the word processor main frame 71. The display apparatus further includes a data electrode drive circuit 200 for driving data electrodes and a signal electrode drive circuit 300 for driving scanning electrodes disposed in the display panel 100 depending on drive data supplied from the display control apparatus 50, and also a temperature sensor 400 disposed at an appropriate position of the display panel 100, e.g., a position providing an average temperature.

The display panel 100 is provided with a display surface 102 including an effective display region 104 and a marginal non-display region 106 formed outside the effective display region 104 on the display surface 102. In this embodiment, electrodes are corresponding to the marginal non-display region 106 are disposed on the display panel 100 and are driven to provide the marginal region.

In display control apparatus 50, a control unit 500, which will be described in detail hereinafter with reference to Figure 10, functions to control the transmission and receipt of various data with the display panel 100 and the word processor main frame 71. A data output unit 600, which will be described in detail with reference to Figure 11, functions to drive the display drive circuits 200 and 300 corresponding to set data from the control unit 500 and start the control unit 500 for data setting based on display data supplied from the word processor main frame 71. A margin drive unit 700 forms the marginal non-display region 106 on the display surface 102 based on output data from the data output unit 600.

A power supply controller 800 appropriately transforms voltage signals from the word processor main frame 71 under the control of the control unit 500 to produce voltages applied to the electrodes through the display drive units 200 and 300. A D/A converter 900 is disposed between the control unit 500 and the power supply controller 800 to convert set digital data from the control unit 500 into analog data and supply the analog data to the power supply controller 800. An A/D converter 950 is disposed between the temperature sensor 400 and the control unit 500 to convert analog temperature data detected at the display

panel 100.

The word processor main frame 71 is a host apparatus functioning as a source of image data supplied to the display panel 100 (through the display control apparatus 50) and can of course be replaced by another form of host apparatus, such as a computer or an image reading apparatus. In this embodiment, the word processor is one capable of supplying and receiving the following data.

Data supplied to the display control apparatus include:

D: image data, address data for designating data display positions, and signals including a horizontal synchronizing signal. Address data for designating display address (corresponding to display positions or pixels on the effective display region 104 for image data) can be outputted from a VRAM corresponding to the effective display region 104, if the host apparatus has such a VRAM. In this embodiment, the word processor main frame 71 supplies such signals in superposition with a horizontal synchronizing signal or flyback erasure signal to the data output unit 600.

CLK: transfer clock pulses for image data PD0 - PD3, supplied to the data output unit 600.

PDOWN: a signal for notifying to break the power supply of the system, supplied to the control unit 500 as a non-maskable interrupting (NMI) signal.

Data supplied from the display control apparatus 50 to the word processor main frame 71 include:

P ON/OFF: status signals for notifying completion of rising and falling of the display control apparatus 50 at the time of turning-on and turning-off of the system power supply, supplied from the control unit 500.

Light: a signal for directing the ON/OFF of a light source FL combined with the display panel 100, supplied from the control unit 500.

Busy: a synchronizing signal for having the word processor main frame 71 delay the transfer of signals in order to allow the display control apparatus 50 to effect various settings at the time of start-up or display operation. In this embodiment, the word processor main frame 71 is constructed so as to be able to receive the "Busy" signal, supplied from the control unit 500 through the data output unit 600.

Figures 8 and 9 are an exploded perspective view and a sectional view, respectively, of an embodiment of a display panel 100 using an FLC. Referring to these figures, the display apparatus 100 comprises an upper glass substrate 110 and a lower glass substrate 120 provided with polarizers (not shown), respectively, forming a pair and arranged in cross nicols. The lower glass substrate 120 is provided with a wired or electrode region 122 comprising transparent electrodes 124 of, e.g., ITO, optionally accompanied with metal electrodes 128 for lowering the resistance formed on the transparent electrodes 124, and an insulating film 120. The metal electrodes 128 need not be added for a small display panel. The upper glass substrate 110 is provided with an electrode region 112 which comprises transparent electrodes 114 and an insulating film 116 similar to the members 124 and 126 of the electrode region 122 formed on the lower glass substrate 120.

The directions of electrode extension of the electrode regions 112 and 122 intersect each other at right angles. In order to provide an effective display region 104 of A5-size, for example, with its longer side disposed in the direction of horizontal scanning, and provide 400 x 800 pixels, each electrode region is provided with 400 or 800 transparent electrodes. In this embodiment, horizontal scanning electrodes (common electrodes) are formed by 400 transparent electrodes 114 disposed to constitute the upper electrode region 112, and data electrodes (segment electrodes) are formed by 800 transparent electrodes 124 to constitute the lower electrode region 122. Further, within the display area 102 and outside the effective display region 104, transparent electrodes 150 are disposed on the upper substrate 110 in the same or different shape compared with the transparent electrodes 114 for data display so as to intersect with extended parts of the transparent electrodes 124 to form a marginal non-display region.

An FLC-filling space 130 is formed between the substrates between the upper substrate 110 and lower substrate 120 and is defined by a pair of alignment films 136 for alignment films 136, spacers 134 for adjusting the gap between the alignment films 136 so as to satisfy a bistability condition and a sealing member 140 of, e.g., an epoxy resin, for sealing the FLC 132. An injection port 142 is formed in the sealing member 140 for injection of the FLC 132 into the filling space 130 and is sealed by a sealing member 144 for sealing the injection port 142 after the injection.

The data electrode drive circuit (segment drive unit) 200 comprises a segment drive element 210 and the scanning electrode drive circuit (common drive circuit) 300 comprises a common drive element 310. The segment drive element 210 and the common drive element 310 respectively comprise 10 and 5 integrated circuits each being used for driving 80 transparent electrodes. The segment and common drive elements 210 and 310 are disposed on substrates 280 and 380, respectively, and are connected through flexible cables 280 and 380, respectively and a connector 299 to the display control apparatus 50 (shown in Figure 7).

Take-out electrodes 115 and 125 are continuously formed with the transparent electrodes 114 and 1 24,

respectively, and are connected through film conductor members 384 and 284 to the drive elements 310 and 210, respectively.

In this embodiment, display is effected by driving the display panel 100 so as to drive the FLC at the respective pixels selectively to the first or second stable state while illuminating the display panel 100 by a light source FL disposed below the lower glass substrate 120.

The display panel 100 of this embodiment as shown in Figures 8 and 9 may be constituted and appropriately controlled for driving while noting the following factors relating to the characteristics of an FLC device.

In constituting a display panel 100 as shown in Figures 8 and 9, a region on a display area or surface 102 corresponding to a region where common-side transparent electrodes 114 and segment-side transparent electrodes 124 are disposed in a matrix is used as a region capable of actually displaying image data, i.e., an effective display region 104. In this instance, in order to make the effective display region 104 completely observable, it is desirable to constitute the display area 102 so as to include at least a part of a region which is outside the region of the common-side transparent electrodes (i.e., scanning electrodes) being disposed in a matrix and is inside the sealing member 140.

However, if only the segment-side transparent electrodes are extended to such a part, the FLC at the part cannot be supplied with an effective electric field for data display but only retains bistable states providing a mixture of transmissive portions (white) and non-transmissive portions (black), whereby not only the beauty of the display is impaired but also such a situation can occur that the definition of the effective display region 104 becomes difficult and an operator is under an optical illusion.

Accordingly, in this embodiment, marginal transparent electrodes 150 are disposed outside the effective display region 104 so as to intersect with the segment-side transparent electrodes 124 and are appropriately be driven to form a marginal region 106. More specifically, e.g., 16 electrodes 150 are disposed on the upper glass substrate 110 on both sides of the region where the common-side transparent electrodes 114 are disposed. In Figure 8, one electrode 150 each is shown as a representative on both sides on the glass substrate 110. Alternatively, one broad marginal transparent electrode can be used instead.

Figure 10 shows an example of the control unit 500, which includes a CPU 501, e.g., in the form of a micro-processor for controlling the respective parts according to a control sequence shown in Figure 12, a ROM 503 developing a program table corresponding to the control sequence shown in Figure 12, and a RAM 505 used for operation during execution of the control sequence by the CPU 501.

PORT1 - PORT6 are port units capable of setting input/output directions and comprise ports P10 - P17, P20 - P27, P30 - P37, P40 - P47, P50 - P57 and P60 - P67, respectively. PORT7 is an output port unit and comprising ports P70 - P74. DDR1 - DDR6 are input/output setting registers (data direction registers) for changing and setting the input/output directions of the ports PORT1 - PORT6, respectively. In this embodiment, some members are not yet used, including: ports P13 - P17 (corresponding to signals A3 - A7) of the port unit PORT1; ports P21 - P25 and P27 of the port unit PORT2; parts P40 and P41 (corresponding to signals A8 and A9, respectively) of the port unit PORT4; ports P53 - P57 of the port unit PORT5; port P62 of the port unit PORT6, ports P72 - P74 of the port unit PORT7; the terminals MPO, MP1 and STBY of the CPU 501.

A reset unit 507 is used to reset the CPU 501, and a clock pulse-generating unit 509 supplies basic clock pulses (4 MHz) for operation to the CPU 501.

TMR1, TMR2 and SCI are timers which are provided with a basic clock pulse generating source and a register, and is capable of frequency-demultiplying the basic clock pulses according to the setting of the register. The timer TMR2 demultiplies the basic clock pulses according to a register setting to provide a system clock signal Tout to the data output unit 600. The data output unit 600 generates a clock signal defining one horizontal scanning period (1H) of the display panel 100 based on the signal 100. The timer TMR1 is used for adjusting the operation periods on the program and the period 1H of the display panel 100 based on a set value for the register.

The timers TMR1 and TMR2 supply an internal interrupting signal IRQ3 to the CPU 501 at the times of completion of the set periods or start of a subsequent time counting following the completion, and the CPU accepts the signal according to necessity.

The timers SCI is not yet used in this embodiment.

Referring further to Figure 10, AB and DB are an address bus and a data bus, respectively, internally connecting the CPU 501 and the respective parts, and 511 denotes a hand shake controller for the port units PORT 5 and PORT 6 with the CPU 501.

Figure 11 shows an example of the data output unit 600, which includes a data input unit 601 which is coupled with the word processor main fame 71 and receives and supplies a signal D and a transfer clock signal CLK. The signal D is supplied from the word processor main frame 71 on receiving image signals

and a horizontal synchronizing signal. In this embodiment, the horizontal scanning signal or horizontal flyback erasure period is supplied in superposition with actual address data. The data input unit 601 charges over data output process depending on detection or non-detection of the horizontal synchronizing signal or horizontal flyback erasure period. More specifically, at the time of detection, the data input unit 601 recognizes the signal component superposed at that time as real or actual address data and outputs the signal as address data RA/D. At the time of non-detection, the signal component is recognized as image data and is outputted as four bits parallel image data D0 - D3.

Further, the data input unit 601 outputs an address/data recognition signal $A/\overline{D}$, and the signal $A/\overline{D}$ is guided to an $\overline{IRQ}$ generating unit 603 and a DACT generating unit 605. On receiving the signal $A/\overline{D}$, the $\overline{IRQ}$ generating unit outputs an interrupting signal $\overline{IRQ}$, which is supplied as an interrupting command $\overline{IRQ1}$ or $\overline{IRQ2}$ to the control unit 500 depending on the setting of a switch 520 (Figure 5), to effect an operation according to a line-access mode or a block-access mode. On the other hand, a DACT generating unit 605 outputs a DACT signal for detecting the access or non-access of the display panel 100 depending on the input of the signal $A/\overline{D}$, and the DACT signal is supplied to the control unit 500, an $\overline{FEN}$ generating unit 611 and a gate array 600.

At the time of energization with the DACT signal, the $\overline{FEN}$ generating unit 611 generates a signal $\overline{FEN}$ for starting the gate array depending on a trigger signal from the $\overline{FEN}$ trigger signal generating unit 613. The $\overline{FEN}$ trigger signal generating unit 613 generates the trigger signal based on a writing signal $\overline{ADWR}$ which is a signal issued by the control unit 500 to command the A/D converter 950 to take in temperature data from the temperature sensor 400. Further, the $\overline{FEN}$ trigger signal generating unit 613 is selected based on a chip selecting signal $\overline{DS0}$ issued by a device selector 621. More specifically, when the control unit 500 selects the A/D converter 950 so as to read the temperature data, the $\overline{FEN}$ trigger signal generating unit 613 is also selected and the margin drive is also started.

A busy gate 619 is also included so as to supply to the word processor main frame 71 a signal BUSY for notifying the busy state of the display control apparatus depending on a busy signal IBUSY from the control unit 500.

The device selector 621 receives signals A10 -A15 from the control unit 500 and, depending on the values thereof, outputs signals $\overline{DS0}$ - $\overline{DS2}$ for selecting the A/D converter 950, D/A converter 900 and data output unit 600. A register selector 623 is started by the signal $\overline{DS2}$ to set a latch pulse gate array 625 based on signals A0 - A4 from the control unit 500. The latch pulse gate array 625 selects the respective registers in a register unit 630 and comprises a number of bits corresponding to the number of registers in the register unit 630. In this embodiment, the register unit 630 comprises 22 register (registers) each of 1 byte (8 bits), and the latch pulse gate array 625 is composed of 22 bits each corresponding to one of the regions. More specifically, when the register selector 623 sets a bit in the latch pulse gate array 625, a register corresponding to the bit is selected and the selected register is subjected to reading or writing of data through a system data bus corresponding to a read signal $\overline{RD}$ or write signal $\overline{WR}$ supplied to the latch pulse gate array 625 from the control unit 500.

In the register unit 630, RA/DL and RA/DU are real address data registers for storing a lower 1 byte and an upper 1 byte of real address data RA/D under the control by a real address storage control unit 641.

DCL and DCU are horizontal dot count data registers for storing a lower 1 byte and an upper 1 byte of data corresponding to a number of dots (800 dots in this embodiment) in the horizontal scanning electrode direction in a display. A horizontal dot number counter 643 is started by the commencement of transfer of image data D0 - D3 to count an appropriate number of clock pulses and lets a latch signal LATH generating unit 645 generate a latch signal when it completes counting numbers equal to those stored in the registers DCL and DCU.

DM is a drive mode register and mode data corresponding to line-access or block access are written therein.

DLL and DLU are registers for common line selection address data and store a lower 1 byte and a higher 1 byte with respect to 16 bit data. Data stored in the register DLL are outputted as address data CA6 and CA5 for designating a block and address data CA4 -CA0 for designating a line. Further, data stored in the register DLU are supplied to a decoder unit 650 and outputted therefrom as chip selection signals $\overline{CS0}$ - $\overline{CS7}$ for selection in the common drive unit 310.

CL1 and CL2 are respectively a region of 1 byte for storing drive data supplied to the common-side drive unit 300 in common-side line drive (line-writing) according to the block access mode. SL1 and SL2 are respectively a region of 1 byte for storing drive data supplied to the segment-side drive unit 200 in segment-side line drive according to the same mode.

CB1 and CB2 are respectively a region of 1 byte for storing drive data supplied to the common-side drive unit 300 in common-side line drive at the time of block erasure according to the block access mode.

SB1 and SB2 are respectively a region of 1 byte for storing drive data supplied to the segment-side drive unit 200 correspondingly.

CC1 and CC2 are respectively a region of 1 byte for storing drive data supplied to common-side drive unit 300 in common-side line drive at the time of line writing according to the line access mode, and SC1 and SC2 are respectively a region of 1 byte for storing drive data supplied to the segment-side drive unit 200 correspondingly.

Subsequent three regions each of 1 byte are regions for storing data for switching by the margin drive unit and they are divided into sub-regions each of 4 bits to provide registers FV_1, FCV_C, FV2, FV3, FSV_C and FV4.

A successive multiplier 661 is used to successively multiply a pulse signal Tout from the control unit 500, e.g., into two times. Ring counters of 3 phases (663A), 4 phases (663B), 6 phases (663C) and 12 phases (663D) are used to count the outputs from the successive multiplier 661 so as to effect division into 1/4, 1/3, 1/2 and 1/1 of one horizontal scanning period (1H). Each of the resultant divided periods is denoted by ΔT hereinafter. In case of the three division (division into 1/3), 1H is constituted by $3\Delta T$.

A multiplexer 665 is used to select any of the outputs from the ring counters 663A - 663D and is actuated depending on the data in the drive mode register DM, i.e., data indicating how many divisions the period 1H is divided into. In case of three divisions for example, the output from the four-phase ring counter 663B is selected.

A 4-phase ring counter 667 is used for the respective outputs from the ring counters 663A - 663D together with a multiplexer 669 which is actuated similarly as the multiplexer 665.

Figure 12 is a flow chart illustrating the outline of display control used in the present invention.

First of all, when the power is turned on to the word processor main frame 71, an INIT routine is automatically started (S101), wherein the "Busy" signal is turned on, the margin display region 106 is driven, the effective display region is erased and the temperature compensation therefor is performed, respectively, at the time of power on, and finely the "Busy" signal is turned off to wait until an interruption request $\overline{IRQ1}$ or $\overline{IRQ2}$ comes. The interruption request $\overline{IRQ1}$ or $\overline{IRQ2}$ is generated by transfer of address data from the main frame 71, and unless the address data come, the display picture 102 remains still.

Then, when the address data are transferred to issue an interruption request, a subsequent step S102 is started. Thus, if the interruption request is $\overline{IRQ1}$, an LSTART routine is started, and if the interruption request is $\overline{IRQ2}$, a BSTART routine is started. According to this branching, it is determined whether the above-mentioned block access or line access is performed. More specifically, the line access is performed if the LSTART routine is started and the block access is started if the BSTART routine is started.

In this embodiment, the setting of $\overline{IRQ1}$ or $\overline{IRQ2}$ is manually performed in advance by a switching means 520 disposed at an appropriate part in the display control apparatus 50.

When the line access mode is set by the switching means and $\overline{IRQ1}$ is generated, the LSTART routine is started and executed, wherein address data transferred from the data output unit are read and judged as to whether the data are for the final line in the effective display region 104 (steps 103 and 104). If the data are not for the final line, the program is branched to start an LLINE routine, wherein the "Busy" signal is turned ON, writing of one scanning line is effected based on image data transferred subsequent to the address data and then the "Busy" signal is turned OFF to wait for an interruption request $\overline{IRQ1}$ (step S105). When $\overline{IRQ1}$ is supplied, the LSTART routine is started again.

In the step S104, if the address data are for the final line, the program is branched to start an FLLINE routine, wherein the writing on the final line is performed based on the transferred image data. Then, the margin display is performed, the temperature compensation data are renewed and the "Busy" signal is turned OFF to wait for an interruption request $\overline{IRQ1}$ (step S106). Then, if the interruption request $\overline{IRQ1}$ is supplied, the LSTART routine is re-started. According to the above-described procedure, the display control according to the line access mode is performed.

On the other hand, if the block access mode is set by the above-mentioned switching means 520, a BSTART routine is started when an interruption request $\overline{IRQ2}$ is generated by transfer of address data. In the routine, "Busy" signal is turned ON, the transferred address data are read to judge whether the data are for the leading line in a block, for the final line in the effective driving region 104 or for other lines (steps S107 and S108).

If the address data do not indicate the leading line or the final line, the program is branched to a LINE routine, wherein writing of one line is performed based on transferred image data and then "Busy" signal is turned OFF to wait for an interruption request (step S109). If an internal interrupting request $\overline{IRQ2}$ is supplied, the BSTART routine is re- started.

In step S108, if the address data indicates the final line in the effective display region 104, an FLINE routine is started. In the routine, writing of one line is performed, the marginal drive is performed, the

temperature compensation data are renewed, and "Busy" signal is turned OFF to wait for an interruption request (step S110). If an interruption request $\overline{IRQ2}$ is supplied, the $\overline{BSTART}$ routine is re-started.

In the step S108, if the address data indicate the leading line of a block, the execution is branched to a BLOCK routine, wherein a block including the lines indicated by the address data is entirely erased into "white" (step S111) and then the LINE routine (step S109) is started to perform similar actions as described above. In the above-described sequence, the display control according to the block access mode is performed to effect data writing.

Further, when the word processor 71 supplies a power down signal PDOWN to the control unit 500, a non-maskable interruption request NM1 is generated by the signal to start a PWOFF routine, wherein "Busy" signal is turned ON, the effective display region 104 is entirely erased into "white". Then, a power status signal and "Busy" signal are turned OFF to shut off the power to the word processor main frame 71.

As is apparent from the above description, even if either of the two modes of display control, i.e., the block access mode and line access mode, is performed, a refresh drive is effected if address data are sequentially transferred cyclically and continuously over the entire effective display region, and a partial rewriting drive is effected if address data for a certain part are transferred intermittently.

In the detailed explanation of control sequence hereinbelow, it is assumed that address data and image data are transferred from the main frame 71 according to the refresh drive mode.

The signals and data transferred between the respective parts used in the above embodiment are summarized as follows:

Signal	Signal name	Supplier	Receiver
Tout	System clock pulse	Control unit 500 (PORT2)	Data output unit 600

(Brief description) Basic clock pulses for operation of the data output unit. Also supplied to the control unit 500 so as to synchronize the time on the control program and the time on the display and always ensure a stable one horizontal scanning period.

$\overline{IRQ1}$	Line-access interruption	Data output unit 600	Control unit 500 (PORT5)
$\overline{IRQ2}$	Block-access interruption	Data output unit 600	Control unit 500 (PORT5)

Either one is supplied to the data control unit 500 depending on an interruption signal IRQ generated by the data output unit 600 based on real address data supplied from the word processor main frame 71.

MR	Memory ready unit	MR generating 500 (PORT5)	Control unit

Signal for timing the access to the D/A controller 900.

$\overline{INTR}$	A/D conversion completion notification	A/D converter 950	Control unit (PORT6)

Signal for notifying that the A/D conversion of detected temperature data has been completed.

IBUSY	Busy	Control unit 500 (PORT6)	Data output unit 600

Supplied to the data output unit 600 so as to notify the word processor main frame 71.

Light	Light source control	Control unit 500 (PORT6)	Main frame 71

Requiring the turning ON/OFF of the light source FL.

P ON/OFF	Power status	Control unit 500 (PORT6)	Main frame 71

Requiring the turning ON/OFF of the power supply.

DACT	Panel access discrimination	Data output unit 600 (DACT generating unit)	Control unit 500 (PORT500) Data output unit 600 (Gate array 680)

Signal for discriminating the access/non-access to the effective display region 104.

$\overline{RD}$	Read signal	Control unit 500 (PORT7)	A/D converter 950 Data output unit 600

Control signal for reading data from the respective input units.

$\overline{WR}$	Write signal	Control unit 500 (PORT7)	A/D converter 950 D/A converter 900 Data output unit 600

Control signal for reading data by the respective units.

DD0 - DD7 A0 - A15	Data on system data bus Address signal	Respective units Control unit 500 (PORT1, PORT4)	Respective units Data output unit 600

Used for having the data output unit 600 select the respective units.

$\overline{RES}$	Reset signal	Control unit 500 (Reset unit 507)	Control unit 500 (CPU 501)

Resetting the CPU 501 in the control unit 500.

$\overline{NMI}$ (PDOWN)	Non-maskable interruption (Power-off interruption)	Main frame 71	Control unit 500 (CPU)

Supplied to the control unit 500 for appropriate actions based on the signal PDOWN from the main frame 71 for notifying power-off.

E	Clock pulses	Control unit 500 (CPU)	D/A converter 900 Data output unit 600

Clock pulses outputted with durations approximately modified depending on the signal for appropriately accessing the D/A converter 900 or data output unit 600.

D0 - D3	Image data	Data output unit 600	Segment-side drive unit 200

Produced from image data as a signal D supplied from the main frame 71.

D	-	Main frame 71	Data output unit 600

Signal including data to be displayed, actual address data and a horizontal synchronizing signal.

CLK	Transfer clock pulses	Main frame 71	Data output unit 600

Transfer clock pulses for the signal D.

A/ $\overline{D}$	Address/data discrimination	Data output unit 600	Data output unit 600

Signal for identifying data supplied as the signal whether they are image data or actual address data.

RA/D	Real address data	Data output unit 600 (Data input unit 601)	Data output unit 600 (Register 630)

Applied to data for specifying the display position. Corresponding to one line and produced from data supplied as the signal D from the main frame 71 in superposition with a horizontal synchronizing signal.

IRQ	Interruption	Data output unit 600	Control unit 500

Supplied to the control unit 500 depending on the signal A/ $\overline{D}$ and supplied to the control unit 500 as $\overline{IRQ1}$ or $\overline{IRQ2}$ depending on the setting.

IRQ3	Internal interruption	Control unit 500 (Timer)	Control unit 500 (CPU)

Internal interruption signal for canceling a non-operative state (sleep state).

$\overline{FEN}$	Frame end	Data output unit 600 ($\overline{FEN}$ generating unit)	Data output unit 600 (Gate array 680)

Used for forming a lateral margin.

$\overline{DS0}$	Chip select	Date output unit 600 (Device selector 621)	A/D converter 950
$\overline{DS1}$			D/A converter 900
$\overline{DS2}$			Data output unit 600 (Register selector 623)
$\overline{DS3}$			Non-use

Generated depending on the signals A10 - A15 from the control unit 500 and used as chip selection signals for the control unit 500.

$\overline{LATH}$	Latch	Data output unit 600	Segment drive unit 200 (Drive element 210)

Signal for latching data (image data) in a shift register in the element 210 into a line memory.

CA0 - CA6	Line selection	Data output unit 600	Common drive unit 300 (Drive element 310)

Signals supplied to the element 310 for selecting horizontal scanning output lines CA5 and CA6 are used for block selection, and CA0 - CA4 are used for selection of lines in a block.

$\overline{CCLR}$	Clearing	Data output unit 600	Common drive unit 300
CEN	Enabling	Data output unit 300	Common drive unit 300
CM1, CM2	Waveform defining	Data output unit 600	Common drive unit 300

Used for defining output waveforms from the common drive element 310.

$\overline{SCLR}$	Clearing	Data output unit 600	Segment drive unit 200
SEN	Enabling	Data output unit 600	Segment drive unit 200
SM1, SM2	Waveform defining	Data output unit 600	Segment drive unit 200

Used for defining output waveforms from the segment drive element 210.

$\overline{V1}$ - $\overline{V4}$ $\overline{CV_C}$ - $\overline{SV_C}$	Margin drive switching	Data output unit 600	Margin drive unit 700

Used for defining outputs from the margin drive unit 700.

V1, V2	Voltage	Power controller 800	Common drive 300

Defining output voltages (two values of opposite polarities) from the element 310.

V3, V4	Voltage	Power controller 800	Segment drive unit 200

Defining output voltages (two values of opposite polarities) from the element 210.

V_C	Voltage	Power controller 800	Drive units 200, 300

Defining the reference level ("0") of the output voltages.

Figure 13 is a diagram for illustrating optimum drive conditions for an FLC at prescribed temperatures. An optimum drive voltage and one horizontal scanning period are controlled by the control unit 500 depending on the temperature data detected by the temperature sensor 400.

In the present invention, the occurrence of flickering in the marginal display region 106 may be suppressed by driving the marginal display region 106 at a frequency of 20 Hz or higher. In this instance, if the environmental temperature varies, the optimum condition for one horizontal scanning period (1H) is changed so that a lower environmental temperature provides a longer 1H period. Accordingly, in the present invention, in order to maintain the driving frequency for the marginal non-display region 106 at 20 Hz or higher, the marginal region is caused to be driven after driving of a prescribed number of scanning electrodes in the display region 104, and the prescribed number is increased at a higher temperature. The counting of the prescribed number of the scanning electrodes is performed in the control unit 500.

Figures 14A and 14B show a set of driving waveforms used in a multi-interlaced drive system (selection with skipping of two or mores scanning electrodes) adopted in the present invention.

More specifically, Fig. 14A shows a scanning selection signal S_{4n-3} (n = 1, 2, 3, ...) applied to a (4n-3)th scanning electrode, a scanning selection signal S_{4n-2} applied to a (4n-2)th scanning electrode, a scanning selection signal S_{4n-1} applied to a (4n-1)th scanning electrode and a scanning selection signal applied to a 4n-th scanning electrode which are respectively applied in a (4M-3)th field F_{4M-3}, a (4M-2)th field F_{4M-2}, a (4M-1)th field F_{4M-1} and a 4Mth field F_{4M} (M = 1, 2, 3...). Herein, one field means one vertical scanning operation or period). According to Fig. 14A, the scanning selection signal S_{4n-3} has voltage polarities (with respect to the voltage level of a scanning non-selection signal) which are opposite to each other in the corresponding phases of the (4M-3)th field F_{4M-3} and (4M-1)th field F_{4M-1}, while the scanning selection signal S_{4n-3} is so composed as to effect no scanning i.e. so as to be a scanning non-selection signal, in the (4M-2)th field F_{4M-2} or 4Mth field F_{4M}. The scanning selection signal S_{4n-1} is similar, but the scanning selection signal S_{4n-3} and S_{4n-1} applied in one field period have different voltage waveforms and have mutually opposite voltage polarities in the corresponding phases.

Similarly, the scanning selection signal S_{4n-2} has voltage polarities (with respect to the voltage level of the scanning non-selection signal) which are mutually opposite in the corresponding phases of the (4M-2)th field F_{4M-2} and 4Mth field F_{4M} and effects no scan in the (4M-3)th field F_{4M-3} or (4M-1)th field F_{4M-1}. The scanning selection signal S_{4n} is similar, but the scanning selection signals S_{4n-2} and S_{4n} applied in one field period have different voltage waveforms and have mutually opposite voltage polarities in the corresponding phases.

Further, in the driving waveform embodiment shown in Figures 14A and 14B, a third phase is disposed for providing a pause to the whole picture (e.g., by applying a voltage of 0 simultaneously to all the pixels constituting the picture), and for this purpose, the scanning selection signals are set to have a voltage of zero (the same voltage level as the scanning non-selection signal).

Referring to Figure 14B, data signals applied to data electrodes in the (4M-3)th field F_{4M-3} comprise a white signal (one for providing a voltages $3V_0$ exceeding a threshold voltage of the FLC at the second phase in combination with the scanning selection signal S_{4n-3} to form a white pixel) and a hold signal (one for applying to a pixel a voltage $\pm V_0$ below the threshold voltage of the FLC in combination with the scanning selection signal S_{4n-3}) which are selectively applied in synchronism with the scanning selection signal S_{4n-3}; and a black signal (for providing a voltage $-3V_0$ exceeding a threshold voltage of the FLC at the second phase in combination with the scanning selection signal S_{4n-1} to form a black pixel) and a hold signal (for applying to a pixel a voltage $\pm V_0$ below the threshold voltage of the ferroelectric liquid crystal in combination with the scanning selection signal S_{4n-1}) which are selectively applied in synchronism with the

scanning selection signal S_{4n-1}. On the contrary, the (4n-2)th scanning electrode and (4n)th scanning electrode are supplied with a scanning non-selection signal, so that the pixels on these scanning electrodes are supplied with the data signals as they are.

In the (4M-2)th field F_{4M-2} subsequent to the writing in the above-mentioned (4M-3)th field F_{4M-3}, data signals applied to the data electrodes comprise the above-mentioned white signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n-2}; and the above-mentioned black signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n}. On the other hand, the (4n-3)th and (4n-1)th scanning electrodes are supplied with a scanning non-selection signal so that the data signals are applied as they are to the pixels on these scanning electrodes.

In the (4M-1)th field F_{4M-1} subsequent to the writing in the above-mentioned (4M-2)th field F_{4M-2}, data signals applied to the data electrodes comprise the above-mentioned black signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n-3}; and the above-mentioned white signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n-1}. On the other hand, the (4n-2)th and (4n)th scanning electrodes are supplied with a scanning non-selection signal so that the data signals are applied as they are to the pixels on these scanning electrodes.

In the 4Mth field F_{4M} subsequent to the writing in the above-mentioned (4M-1)th field F_{4M-1}, data signals applied to the data electrodes comprise the above-mentioned black signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n-2}; and the above- mentioned white signal and hold signal which are selectively applied in synchronism with the scanning selection signal S_{4n}. On the other hand, the (4n-3)th and (4n-1)th scanning electrodes are supplied with a scanning non-selection signal so that the data signals are applied as they are to the pixels on these scanning electrodes.

Figures 15A, 15B and 15C are time charts showing successions of driving waveforms shown in Figures 6A and 6B used for writing to form a display state shown in Figure 15D. In Figure 15D, o denotes a pixel written in white and ● denotes a pixel written in black. Further, referring to Figure 15B, at I_1 - S_1 is shown a time-serial voltage waveform applied to the intersection of a scanning electrode S1 and a data electrode I_1. At I_2 - S_1 is shown a time-serial waveform applied to the intersection of the scanning electrode S_1 and a data electrode I_2. Similarly, at I_1 - S_2 is shown a time-serial voltage waveform applied to the intersection of a scanning electrode S_2 and the data electrode I_1; and at I_2 - S_2 is shown a time-serial voltage waveform applied to the intersection of the scanning electrode S_2 and the data electrode I_2.

The driving scheme which may be suitably adopted in the present invention is not restricted to the one described above. For example, the selection of scanning electrodes may be effected every fourth, fifth, sixth, seventh, eighth or less frequently in each field. Every eighth or less frequent scanning (i.e., scanning with seven or more electrodes apart) is preferred. Further, the scanning selection signal may be polarity-inverted for each field as shown in Figure 14A but may also be consistent throughout a frame including plural fields or throughout a display operation.

Referring to Figure 16, there is schematically shown an example of a ferroelectric liquid crystal cell. Reference numerals 141a and 141b denote substrates (glass plates) on which a transparent electrode of, e.g., In_2O_3, SnO_2, ITO (Indium-Tin-Oxide), etc., is disposed, respectively. A liquid crystal of an SmC*-phase in which liquid crystal molecular layers 142 are oriented perpendicular to surfaces of the glass plates is hermetically disposed therebetween. A full line 143 shows liquid crystal molecules. Each liquid crystal molecule 143 has a dipole moment ($P_\perp$) 144 in a direction perpendicular to the axis thereof. When a voltage higher than a certain threshold level is applied between electrodes formed on the base plates 141a and 141b, a helical or spiral structure of the liquid crystal molecule 143 is unwound or released to change the alignment direction of respective liquid crystal molecules 143 so that the dipole moment ($P_\perp$) 144 are all directed in the direction of the electric field. The liquid crystal molecules 143 have an elongated shape and show refractive anisotropy between the long axis and the short axis thereof. Accordingly, it is easily understood that when, for instance, polarizers arranged in a cross nicol relationship, i.e., with their polarizing directions crossing each other, are disposed on the upper and the lower surfaces of the glass plates, the liquid crystal cell thus arranged functions as a liquid crystal optical modulation device of which optical characteristics vary depending upon the polarity of an applied voltage. Further, when the thickness of the liquid crystal cell is sufficiently thin (e.g., 1 micron), the helical structure of the liquid crystal molecules is released without application of an electric field whereby the dipole moment assumes either of the two states, i.e., Pa in an upper direction 154a or Pb in a lower direction 154b, thus providing a bistability condition, as shown in Figure 17. When an electric field Ea or Eb higher than a certain threshold level and different from each other in polarity as shown in Figure 17 is applied to a cell having the above-mentioned characteristics, the dipole moment is directed either in the upper direction 154a or in the lower direction 154b depending on the vector of the electric field Ea or Eb. In correspondence with this, the liquid crystal molecules are oriented to either a first orientation state 153a or a second orientation state 153b.

When the above-mentioned ferroelectric liquid crystal is used as an optical modulation element, it is possible to obtain two advantages. First is that the response speed is quite fast. Second is that the orientation of the liquid crystal shows bistability. The second advantage will be further explained, e.g., with reference to Figure 17. When the electric field Ea is applied to the liquid crystal molecules, they are oriented in the first stable state 153a. This state is stably retained even if the electric field is removed. On the other hand, when the electric field Eb of which direction is opposite to that of the electric field Ea is applied thereto, the liquid crystal molecules are oriented to the second orientation state 153b, whereby the directions of molecules are changed. Likewise, the latter state is stably retained even if the electric field is removed. Further, as long as the magnitude of the electric field Ea or Eb being applied is not above a certain threshold value, the liquid crystal molecules are placed in the respective orientation states. In order to effectively realize high response speed and bistability, it is preferable that the thickness of the cell is as thin as possible and generally 0.5 to 20 microns, particularly 1 to 5 microns.

In the present invention, in addition to the specific driving embodiments described above, there may also be applied driving schemes as disclosed in, e.g., U.S. Patents Nos. 4548476, 4655561, 4697887, 4709995, 4712872 and 4747671. Further, the liquid crystal panel suitably used in the present invention may be a ferroelectric liquid crystal panel as disclosed in U.S. Patents Nos. 4639089, 4674839, 4682858, 4709994, 4712873, 4712874, 4712875, 4712877 and 4714323.

As described above, according to the present invention, it has become possible to suppress or remove flickering due to change in contrast occurring in a drive scheme which uses a limited region for display in order to provide an improved image quality. Further, according to the present invention, it has become possible to suppress the occurrence of flickering in a marginal display region accompanying a change in environmental temperature.

A display apparatus includes: (a) a liquid crystal device comprising scanning electrodes, data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes, the scanning electrodes and data electrodes being disposed to intersect each other so as to form an electrode matrix and provide a display surface covering the electrode matrix, (b) first means for applying a scanning selection signal to the scanning electrodes and applying data signals to the data electrodes in synchronism with the scanning selection signal, and (c) second means for dividing the display surface into an effective display region and a non-display region and controlling the first means so as to apply a scanning selection signal to a scanning electrode covered by the non-display region in a shorter cycle than the application of a scanning selection signal to scanning electrodes covered by the effective display region.

Claims

1. A display apparatus, comprising:

(a) a liquid crystal device comprising scanning electrodes, data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes, the scanning electrodes and data electrodes being disposed to intersect each other so as to form an electrode matrix and provide a display surface covering the electrode matrix,

(b) first means for applying a scanning selection signal to the scanning electrodes and applying data signals to the data electrodes in synchronism with the scanning selection signal, and

(c) second means for dividing the display surface into an effective display region and a non-display region and controlling the first means so as to apply a scanning selection signal to a scanning electrode covered by the non-display region in a shorter cycle than the application of a scanning selection signal to scanning electrodes covered by the effective display region.

2. An apparatus according to Claim 1, wherein the scanning electrode covered by the non-display region is disposed outside the scanning electrodes covered by the display region and is set to have a larger width than a scanning electrode covered by the display region.

3. A display apparatus, comprising:

(a) a liquid crystal device comprising scanning electrodes, data electrodes and a ferroelectric liquid crystal disposed between the scanning electrodes and data electrodes, the scanning electrodes and data electrodes being disposed to intersect each other so as to form an electrode matrix and provide a display surface covering the electrode matrix,

(b) first means for applying a scanning selection signal to the scanning electrodes and applying data signals to the data electrodes in synchronism with the scanning selection signal, and

(c) second means for dividing the display surface into an effective display region covering a total of M scanning electrodes and a non-display region covering a scanning electrode and controlling the first

means so as to apply a scanning selection signal to the scanning electrodes in the display region in such a manner that a scanning selection signal is applied to the scanning electrodes N electrodes apart (N: an integer of 1 or more) in one scanning operation and applied to all the M scanning electrodes covered by the display region in N+1 times of scanning operation, and to apply a scanning selection signal to the scanning electrode covered by the non-display region in a cycle during which the scanning selection signal is applied to M or less scanning electrodes in the display region.

4. An apparatus according to Claim 3, wherein the scanning selection signal is applied to the scanning electrode covered by the non-display region in a cycle during which the scanning selection signal is applied to M/(N+1) or less scanning electrodes in the display region.

5. An apparatus according to Claim 3, wherein the scanning selection signal is applied to the scanning electrode covered by the non-display region in a cycle during which the scanning selection signal is applied to M/2(N+1) or less scanning electrodes in the display region.

6. An apparatus according to Claim 3, wherein the scanning electrode covered by the non-display region is disposed outside the scanning electrodes covered by the display region and is set to have a larger width than a scanning electrode covered by the display region.

7. A display apparatus, comprising:

(a) a display panel comprising scanning electrodes and data electrodes disposed to intersect the scanning electrodes so as to form a pixel at each intersection, and including a display region comprising a plurality of the pixels arranged in a plurality of rows and a plurality of columns and a marginal non-display region disposed outside the display region and constituted by a third electrode which is disposed in parallel with the scanning electrodes,

(b) drive means including a scanning electrode drive means for supplying a scanning signal to the scanning electrodes, a data electrode drive means for supplying data signals so as to form an image in the display region, and a marginal display drive means for supplying a voltage signal to the third electrode so as to form either one of a bright state and a dark state at the marginal non-display region, and

(c) control means for controlling the drive means so as to apply the voltage signal to the third electrode each time after the scanning signal is supplied to a prescribed number of scanning electrodes and to increase the prescribed number corresponding to an increase in environmental temperature.

8. An apparatus according to Claim 7, wherein said display panel includes a liquid crystal disposed between the scanning electrodes and data electrodes.

9. An apparatus according to Claim 8, wherein said liquid crystal is a ferroelectric liquid crystal.

10. A display apparatus, comprising:

(a) a display panel comprising first electrodes and second electrodes disposed to intersect the first electrodes so as to form pixels arranged in a plurality of rows and a plurality of columns, each pixel being formed at an intersection of the first electrodes and the second electrodes,

(b) first electrode drive means for supplying a scanning signal to the first electrodes,

(c) second electrode drive means for supplying data signals to the second electrodes in synchronism with the scanning signal, and

(d) control means for controlling the first electrode drive means and the second electrode drive means so that:

the pixels are divided to form a display region and a non-display region outside the display region,

a scanning signal is applied to first electrodes constituting the display region and a voltage signal is applied to a first electrode constituting the non-display region so as to form an image corresponding to given image data in the display region and form either one of a bright state and a dark state, and

the voltage signal is applied to the first electrode constituting the non-display region each time after the scanning signal is applied to prescribed number of the first electrodes constituting the display region, and the prescribed number is changed corresponding to a change in environmental temperature.

11. An apparatus according to Claim 10, wherein said display panel includes a liquid crystal disposed between the first electrodes and the second electrodes.

12. An apparatus according to Claim 10, wherein said prescribed number of the first electrodes is increased corresponding to an increase in environmental temperature.

13. A display apparatus, comprising:

(a) a display panel comprising scanning electrodes and data electrodes disposed to intersect the scanning electrodes so as to form a pixel at each intersection, and including a display region comprising a plurality of the pixels arranged in a plurality of rows and a plurality of columns and a marginal non-display region disposed outside the display region and constituted by a third electrode which is disposed in parallel with the scanning electrodes,

(b) first drive means for applying a scanning selection signal to the scanning electrodes in a total

number of M corresponding to the display region in such a manner that a scanning selection signal is applied to the scanning electrodes N electrodes apart (N: an integer of 1 or more) in one scanning operation and applied to all the M electrodes in the display region in N+1 times of scanning operation, and applying a voltage signal to the third electrode corresponding to the non-display region in a cycle during which the scanning selection signal is applied to a prescribed number of M or less scanning electrodes in the display region,

(c) second drive means for applying data signals to the data electrodes so as to display an image in the display region and display either one of a bright state and a dark state in the non-display region, and

(d) control means for controlling the first and second drive means so that the prescribed number of M or less is increased corresponding to an increase in environmental temperature.

14. An apparatus according to Claim 13, wherein said display panel includes a liquid crystal disposed between the scanning electrodes and data electrodes.

15. An apparatus according to Claim 14, wherein said liquid crystal is a ferroelectric liquid crystal.

16. A display apparatus, comprising:

(a) a display panel comprising first electrodes and second electrodes disposed to intersect the first electrodes so as to form pixels arranged in a plurality of rows and a plurality of columns, each pixel being formed at an intersection of the first electrodes and the second electrodes,

(b) first electrode drive means for supplying a scanning signal to the first electrodes,

(c) second electrode drive means for supplying data signals to the second electrodes in synchronism with the scanning signal, and

(d) control means for controlling the first electrode drive means and the second electrode drive means so that:

the pixels are divided to form a display region and a non-display region outside the display region,

a scanning signal is applied to first electrodes constituting the display region and a voltage signal is applied to a first electrode constituting the non-display region so as to form an image corresponding to given image data in the display region and form either one of a bright state and a dark state, and

a scanning selection signal is applied to first electrodes in a total number of M corresponding to the display region in such a manner that a scanning selection signal is applied to the first electrodes N electrodes apart (N: an integer of 1 or more) in one scanning operation and applied to all the M electrodes in the display region in N+1 times of scanning operation, and a voltage signal is applied to the first electrode corresponding to the non-display region in a cycle during which the scanning selection signal is applied to a prescribed number of M or less first electrodes in the display region,

the voltage signal is applied to the first electrode constituting the non-display region each time after the scanning signal is applied to prescribed number of the first electrodes constituting the display region, and the prescribed number is changed corresponding to a change in environmental temperature.

17. An apparatus according to Claim 16, wherein said display panel includes a liquid crystal disposed between the first electrodes and second electrodes.

18. An apparatus according to Claim 17, wherein said liquid crystal is a ferroelectric liquid crystal.

19. An apparatus according to Claim 16, wherein said prescribed number of the first electrodes is increased corresponding to an increase in environmental temperature.

20. A display apparatus, comprising:

(a) a display panel comprising first electrodes and second electrodes disposed to intersect the first electrodes so as to form pixels arranged in a plurality of rows and a plurality of columns, each pixel being formed at an intersection of the first electrodes and the second electrodes,

(b) first electrode drive means for supplying a scanning signal to the first electrodes,

(c) second electrode drive means for supplying data signals to the second electrodes in synchronism with the scanning signal, and

(d) control means for controlling the first electrode drive means and the second electrode drive means so that:

the pixels are divided to form a display region and a non-display region outside the display region,

a scanning signal is applied to first electrodes constituting the display region and a voltage signal is applied to a first electrode constituting the non-display region so as to form an image corresponding to given image data in the display region and form either one of a bright state and a dark state, and

the number of the application of the scanning signal to the first electrodes constituting the display region is counted, and after a prescribed number is counted, the application of the voltage signal to the first electrode constituting the non-display region is started.

21. An apparatus according to Claim 20, wherein said display panel includes a liquid crystal disposed between the first electrodes and the second electrodes.

22. An apparatus according to Claim 21, wherein said liquid crystal is a ferroelectric liquid crystal.

23. An apparatus according to Claim 20, wherein said prescribed number is changed corresponding to a change in environmental temperature.

24. An apparatus according to Claim 20, wherein said prescribed number is increased corresponding to an increase in environmental temperature.

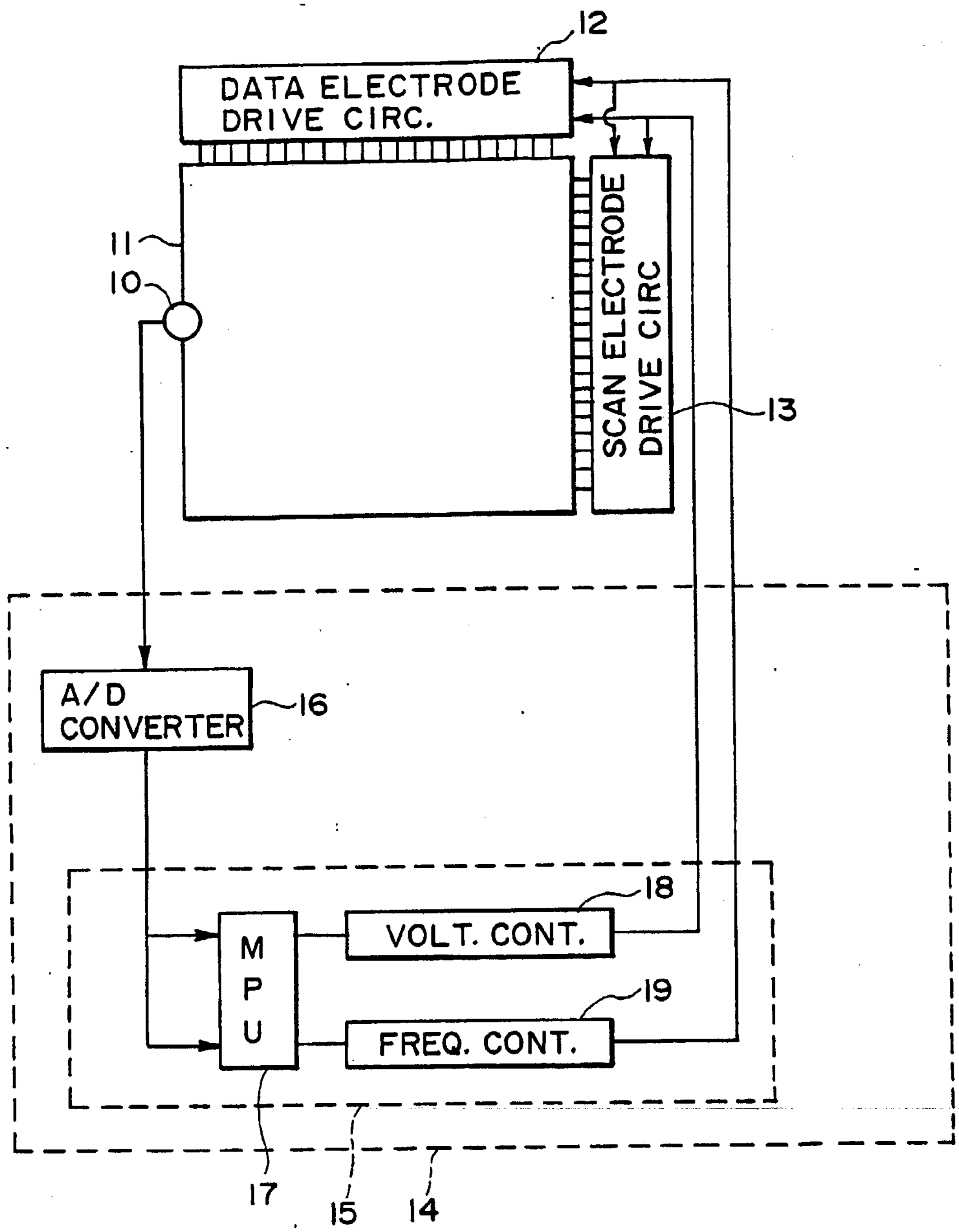

12
DATA ELECTRODE DRIVE CIRC.
11
10
SCAN ELECTRODE DRIVE CIRC
13
A/D CONVERTER
16
18
M P U
VOLT. CONT.
19
FREQ. CONT.
17
15
14

FIG. 1

16.08.89

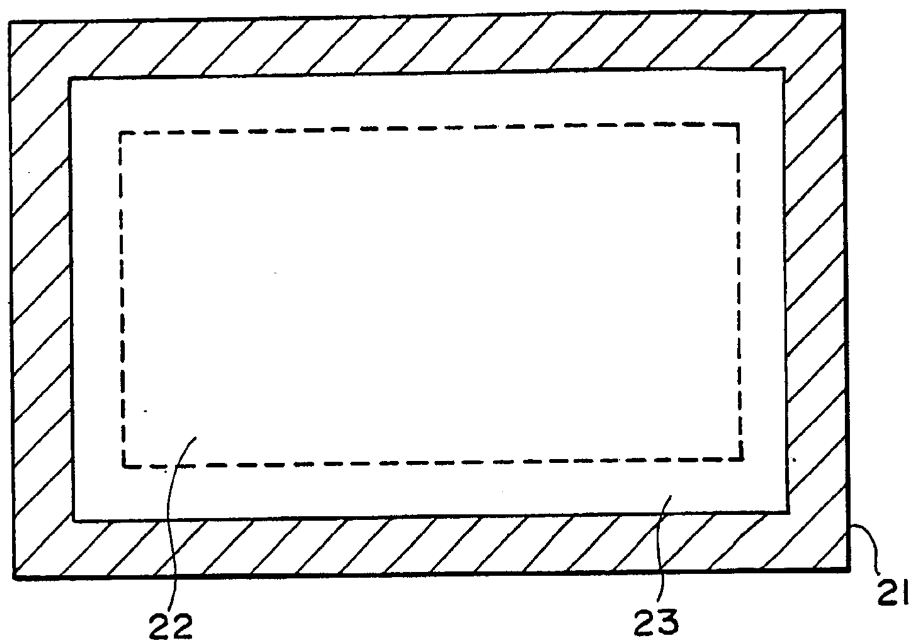


FIG. 2

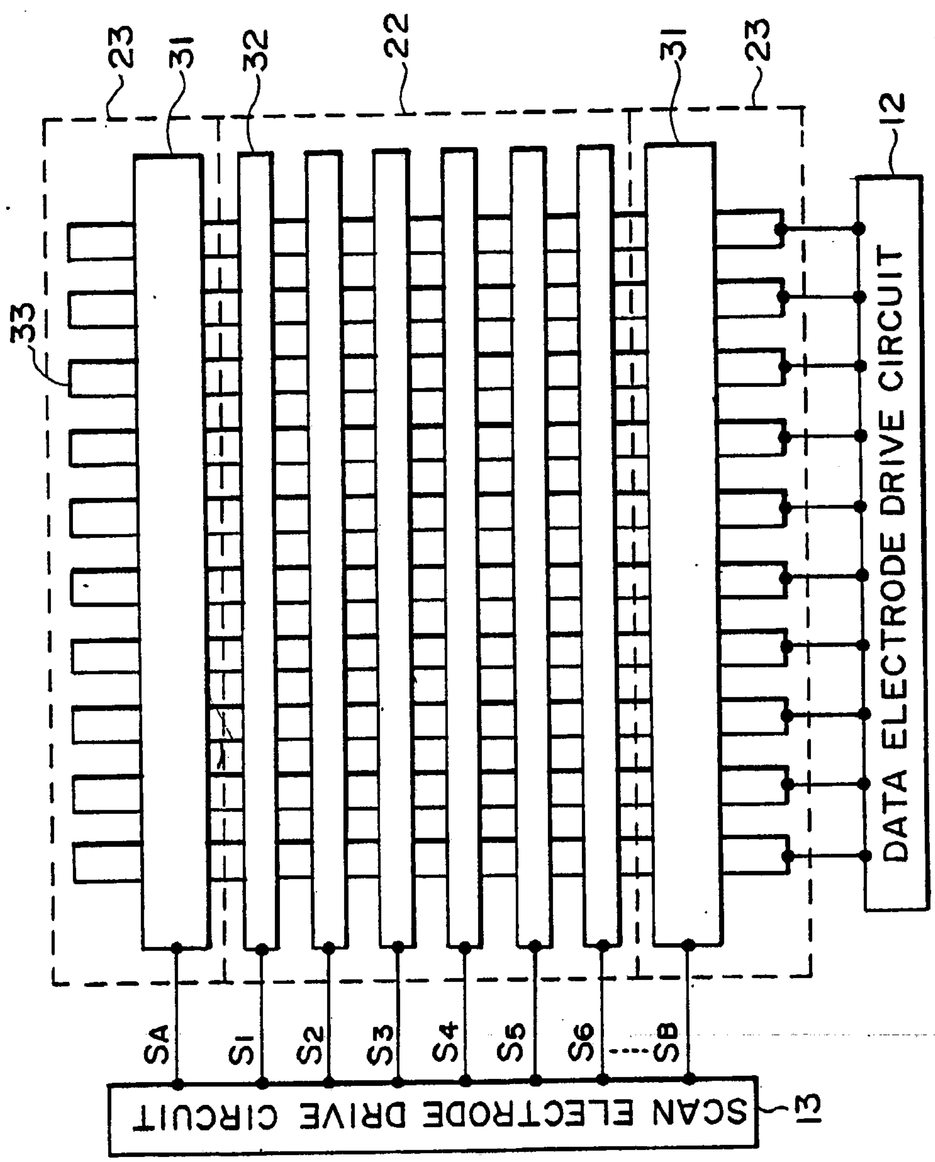
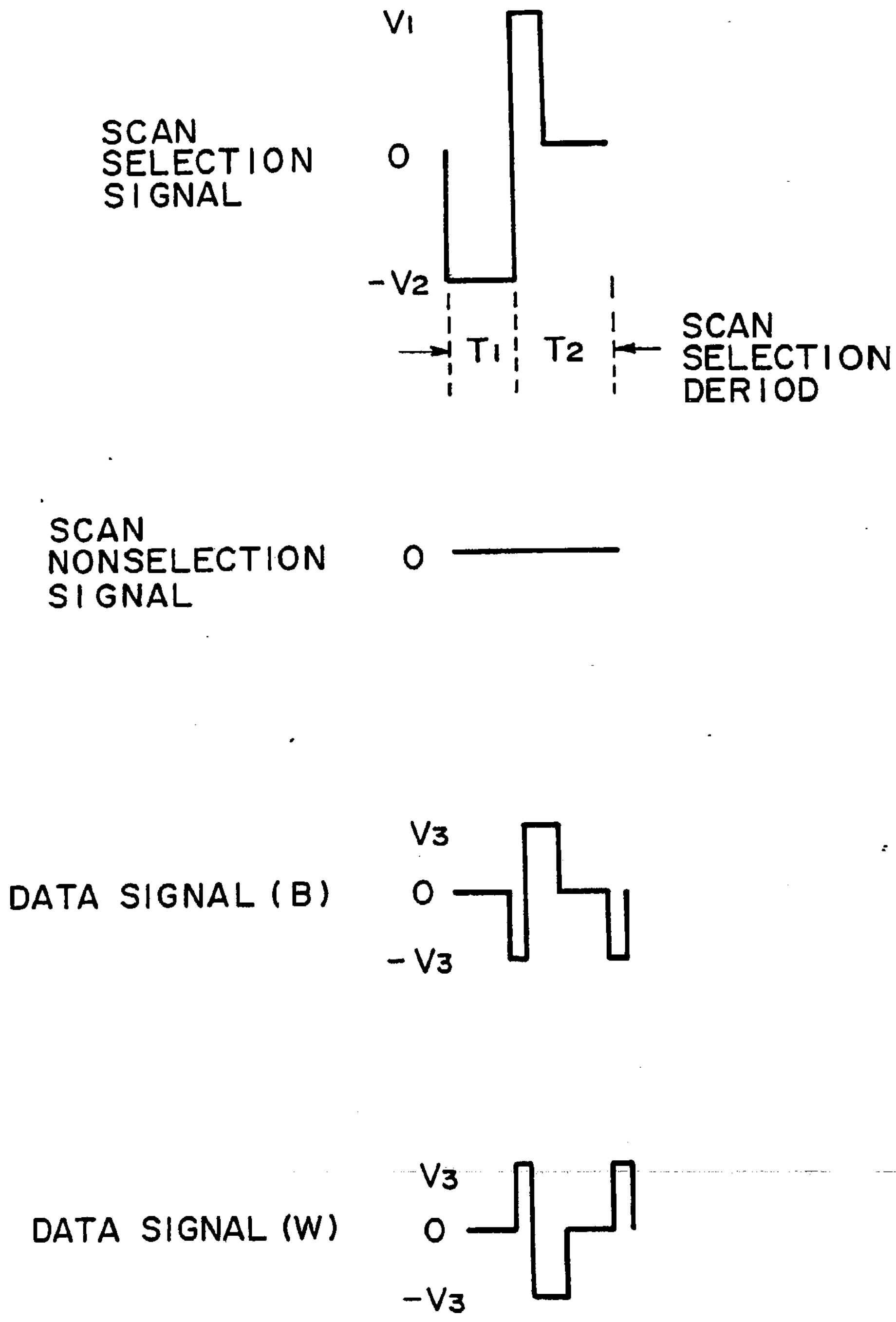

23
31
32
22
31
23
33
12
DATA ELECTRODE DRIVE CIRCUIT
SA
S1
S2
S3
S4
S5
S6
SB
SCAN ELECTRODE DRIVE CIRCUIT
13

FIG. 3

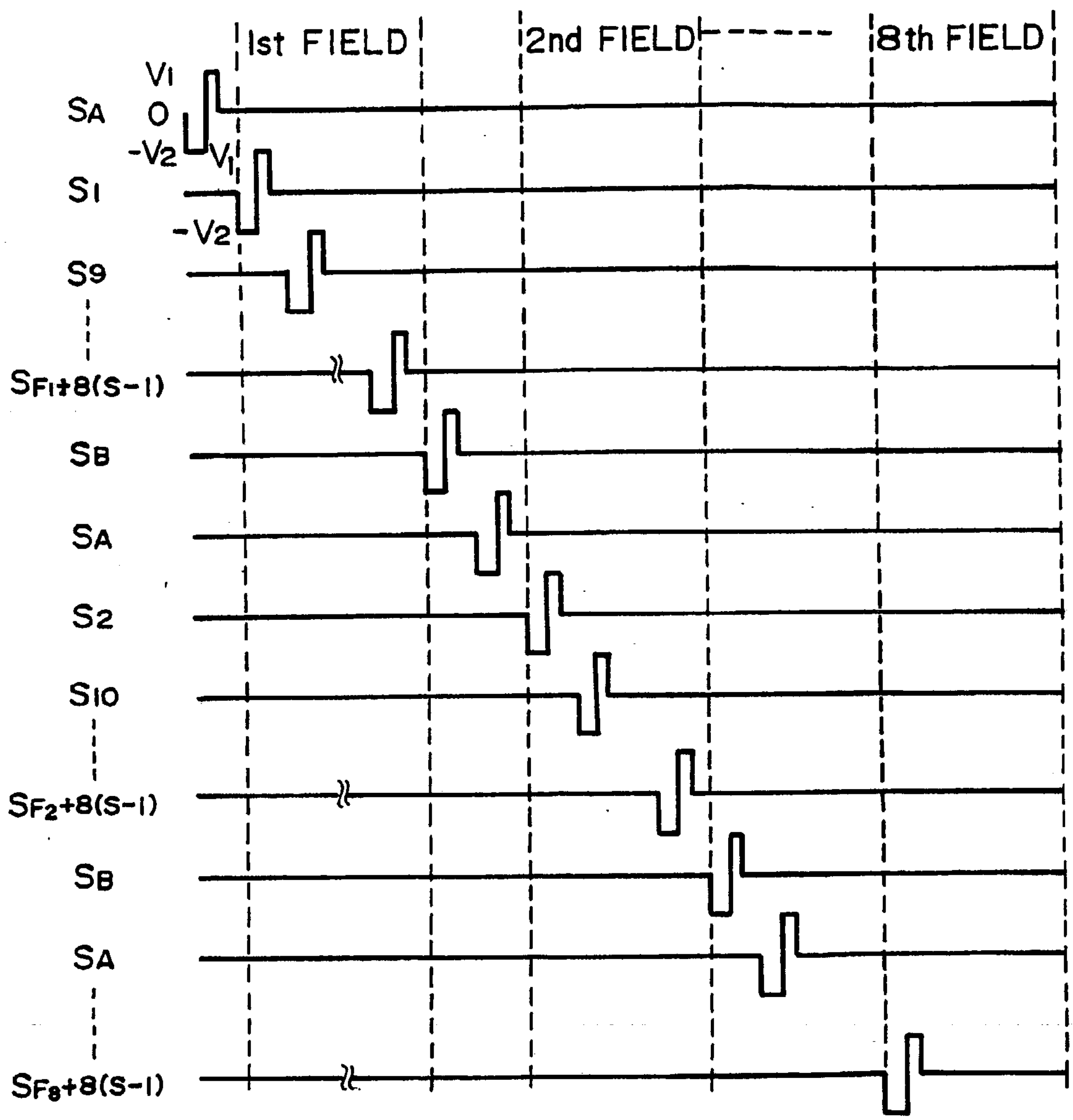
15.08.89



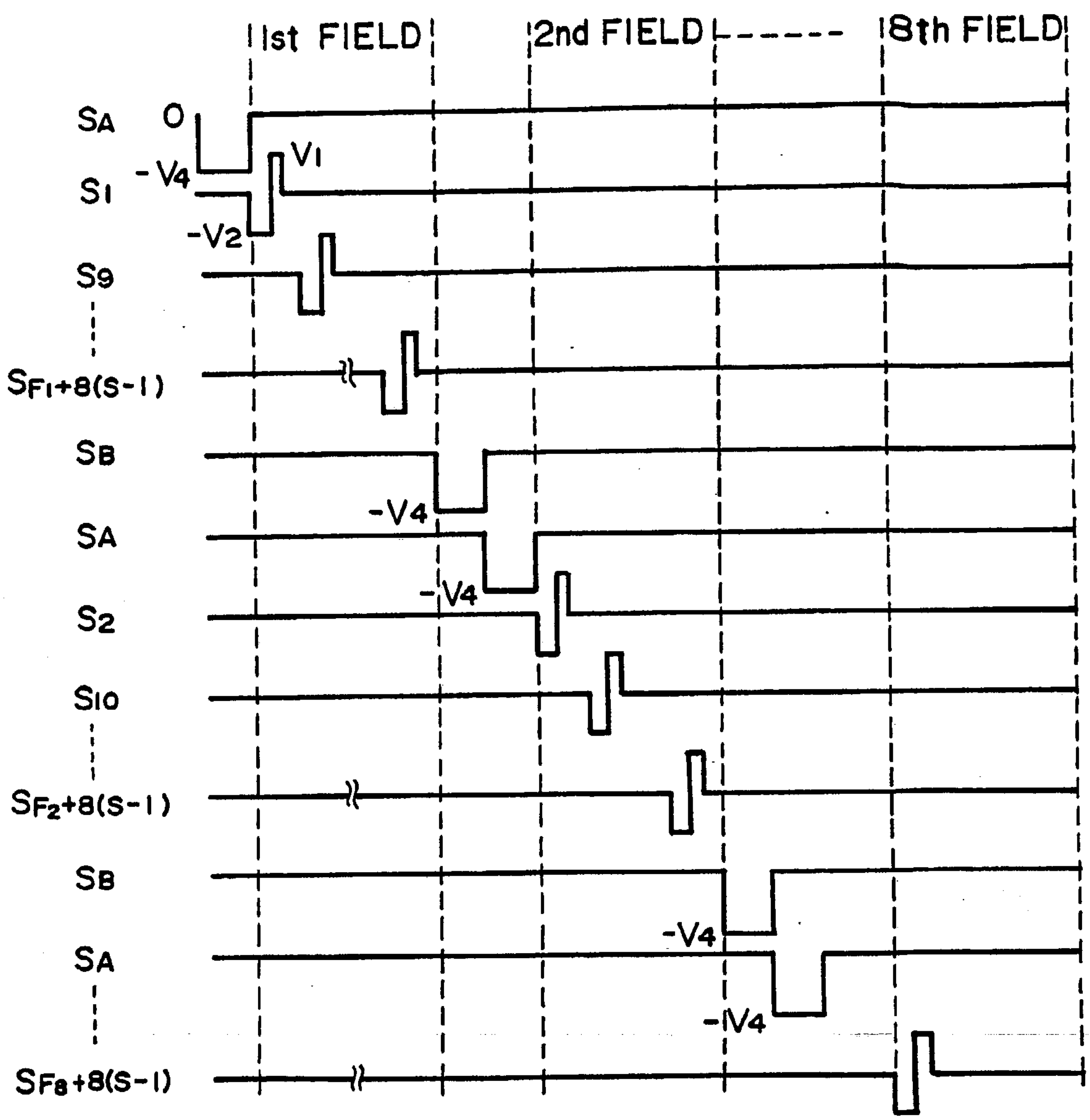
V1
SCAN SELECTION SIGNAL
0
-V2
T1
T2
SCAN SELECTION DERIOD
SCAN NONSELECTION SIGNAL
0
V3
DATA SIGNAL (B)
0
-V3
V3
DATA SIGNAL (W)
0
-V3

F I G. 4

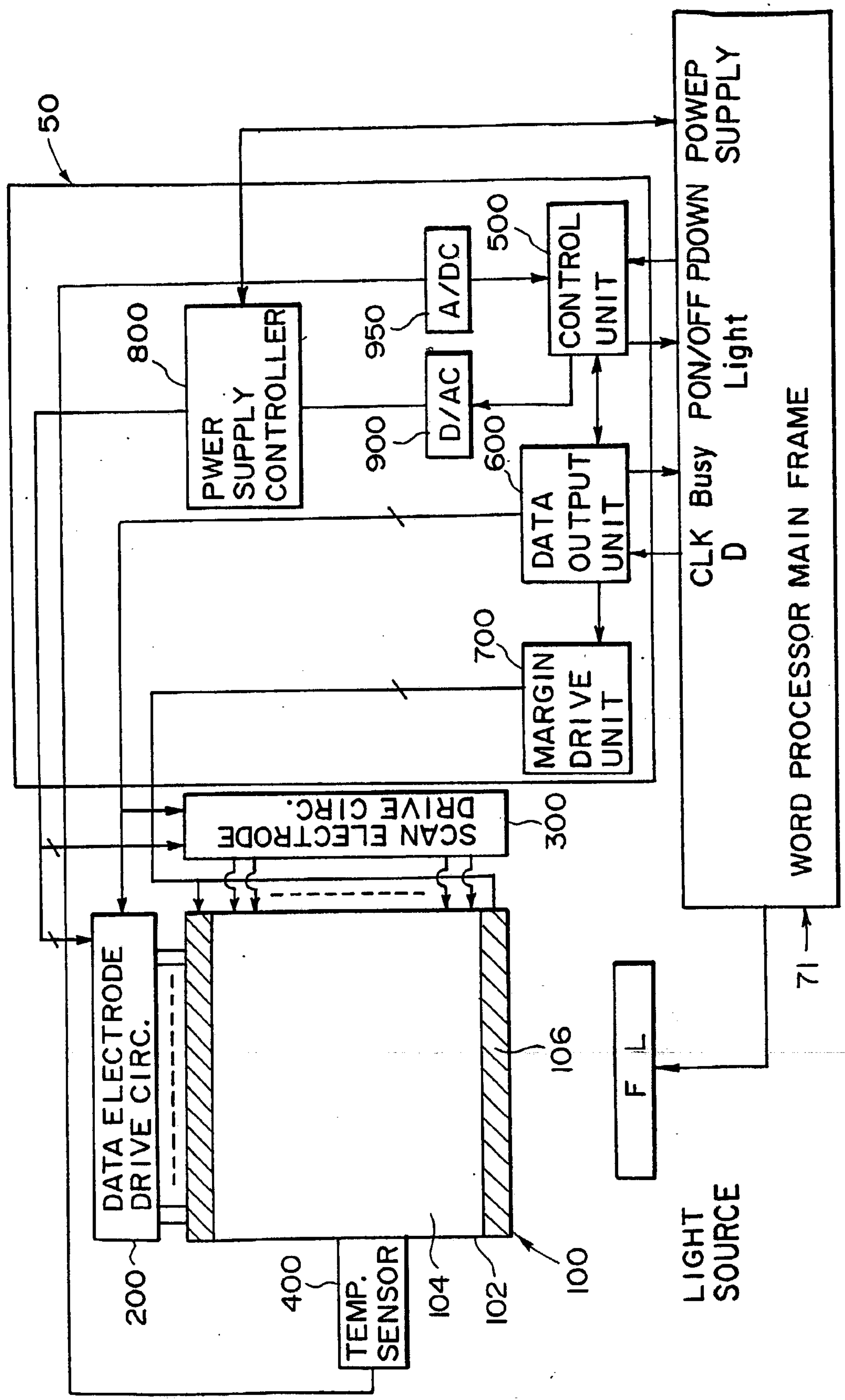
16·08·89


1st FIELD
2nd FIELD
8th FIELD
V1
0
-V2
SA
S1
S9
SF1+8(S-1)
SB
SA
S2
S10
SF2+8(S-1)
SB
SA
SF8+8(S-1)

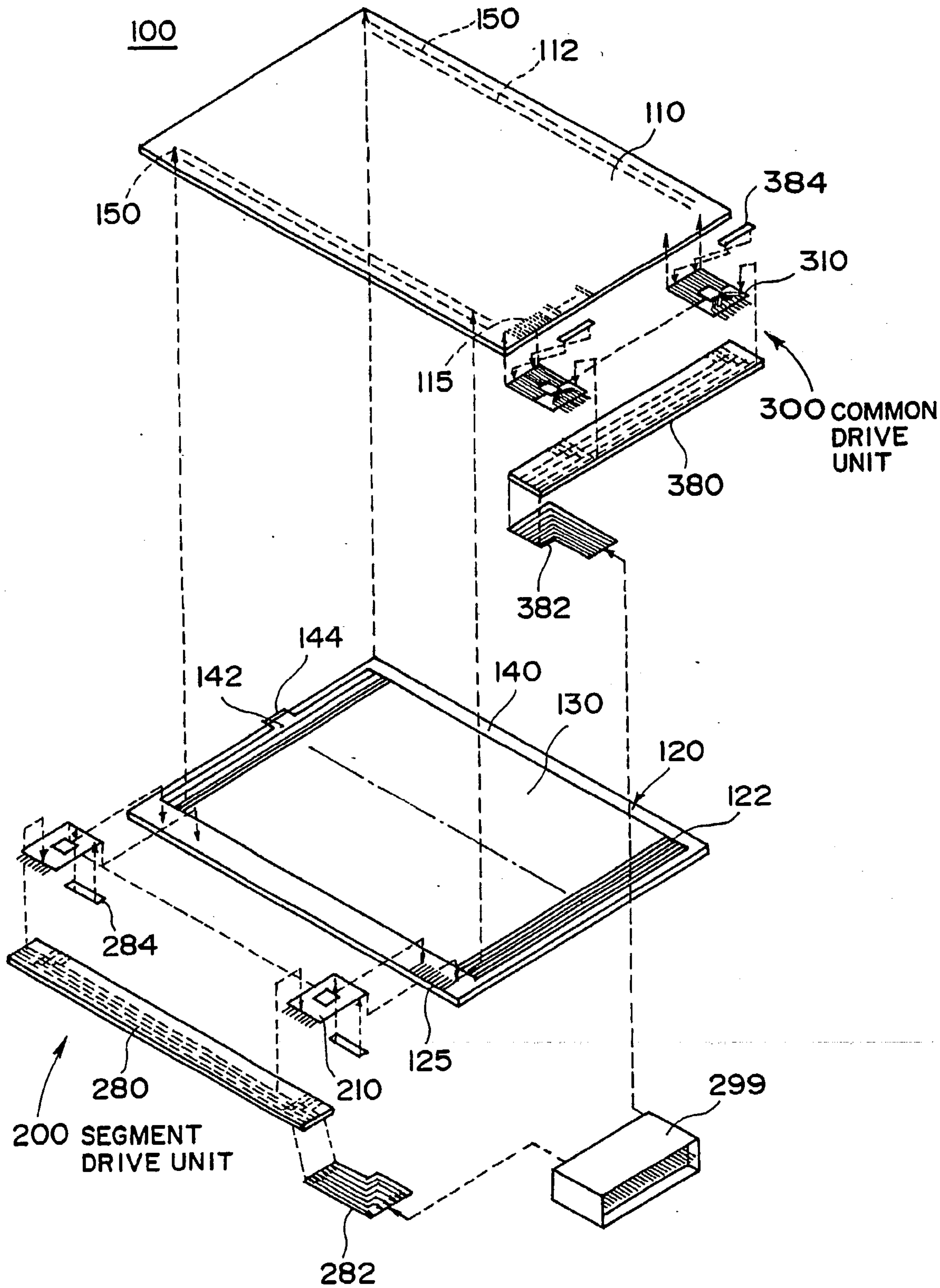
F I G. 5


1st FIELD
2nd FIELD
8th FIELD
SA
0
-V4
V1
S1
-V2
S9
SF1+8(S-1)
SB
-V4
SA
-V4
S2
S10
SF2+8(S-1)
SB
-V4
SA
-V4
SF8+8(S-1)

F I G. 6


50
POWEP SUPPLY
PON/OFF PDOWN
Light
CLK Busy
D
WORD PROCESSOR MAIN FRAME
500
CONTROL UNIT
A/DC
950
800
PWER SUPPLY CONTROLLER
D/AC
900
600
DATA OUTPUT UNIT
700
MARGIN DRIVE UNIT
SCAN ELECTRODE DRIVE CIRC.
300
DATA ELECTRODE DRIVE CIRC.
200
400
TEMP. SENSOR
104
102
100
106
F L
71
LIGHT SOURCE

F I G. 7


100
150
112
110
150
384
310
115
300 COMMON DRIVE UNIT
380
382
144
142
140
130
120
122
284
280
210
125
299
200 SEGMENT DRIVE UNIT
282

F I G. 8

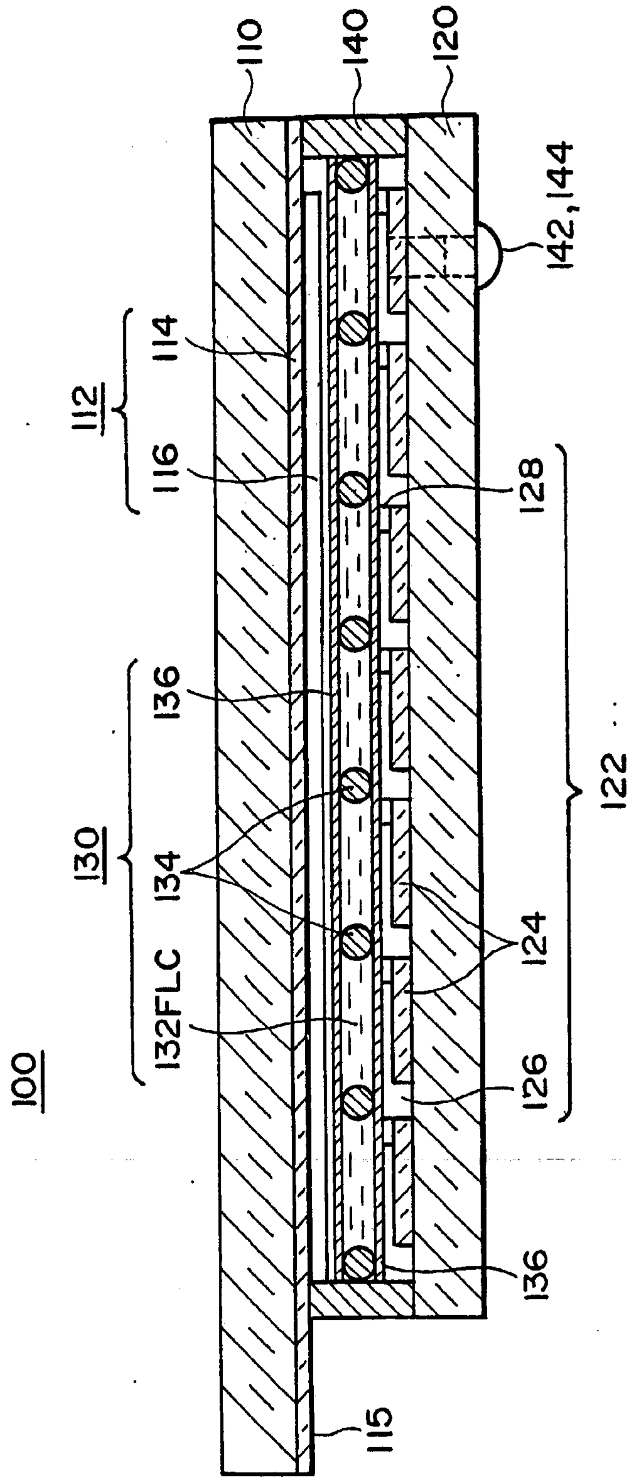
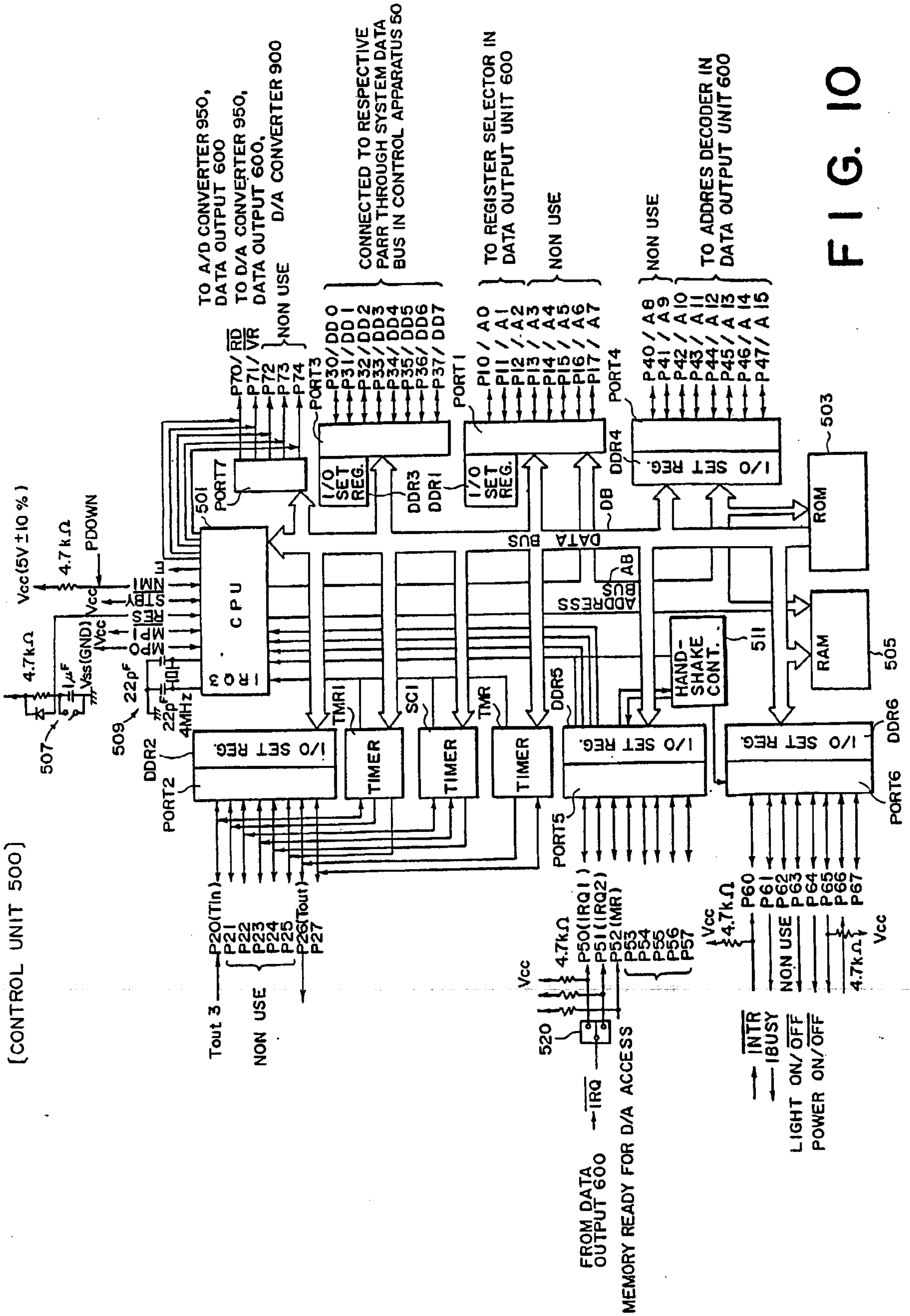

110
140
120
142,144
112
114
116
128
130
136
134
132FLC
124
126
122
100
136
115

FIG. 9


[CONTROL UNIT 500]
CPU
ROM
RAM
HAND-SHAKE CONT.
TIMER
I/O SET REG.
DATA BUS
ADDRESS BUS
PORT1
PORT2
PORT3
PORT4
PORT5
PORT6
PORT7
TO A/D CONVERTER 950, DATA OUTPUT 600
TO D/A CONVERTER 950, DATA OUTPUT 600, D/A CONVERTER 900
NON USE
CONNECTED TO RESPECTIVE PARR THROUGH SYSTEM DATA BUS IN CONTROL APPARATUS 50
TO REGISTER SELECTOR IN DATA OUTPUT UNIT 600
TO ADDRES DECODER IN DATA OUTPUT UNIT 600
FROM DATA OUTPUT 600
MEMORY READY FOR D/A ACCESS
LIGHT ON/OFF
POWER ON/OFF
Vcc(5V ±10 %)
PDOWN
4MHz

F I G. 10

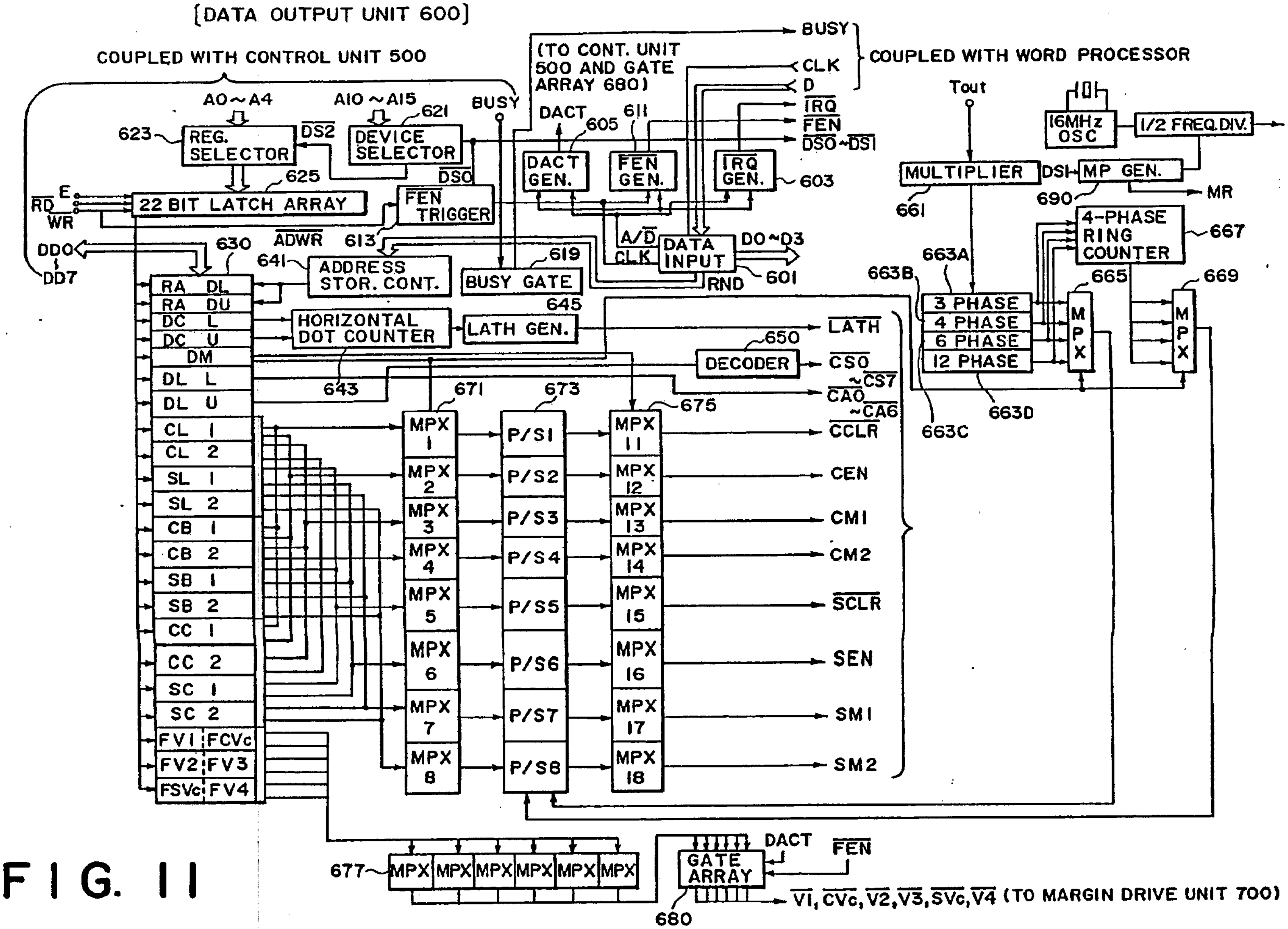

[DATA OUTPUT UNIT 600]
COUPLED WITH CONTROL UNIT 500
COUPLED WITH WORD PROCESSOR
(TO CONT. UNIT 500 AND GATE ARRAY 680)
BUSY
CLK
D
IRQ
FEN
DSO~DSI
A0~A4
A10~A15
REG. SELECTOR
DEVICE SELECTOR
22 BIT LATCH ARRAY
FEN TRIGGER
DACT GEN.
FEN GEN.
IRQ GEN.
DATA INPUT
A/D
CLK
D0~D3
RND
ADDRESS STOR. CONT.
BUSY GATE
HORIZONTAL DOT COUNTER
LATH GEN.
DECODER
LATH
CS0~CS7
CA0~CA6
CCLR
CEN
CM1
CM2
SCLR
SEN
SM1
SM2
Tout
MULTIPLIER
16MHz OSC
1/2 FREQ.DIV.
MP GEN.
MR
4-PHASE RING COUNTER
3 PHASE
4 PHASE
6 PHASE
12 PHASE
MPX
RA DL
RA DU
DC L
DC U
DM
DL L
DL U
CL 1
CL 2
SL 1
SL 2
CB 1
CB 2
SB 1
SB 2
CC 1
CC 2
SC 1
SC 2
FV1 FCVc
FV2 FV3
FSVc FV4
MPX 1
MPX 2
MPX 3
MPX 4
MPX 5
MPX 6
MPX 7
MPX 8
P/S1
P/S2
P/S3
P/S4
P/S5
P/S6
P/S7
P/S8
MPX 11
MPX 12
MPX 13
MPX 14
MPX 15
MPX 16
MPX 17
MPX 18
GATE ARRAY
DACT
V1, CVc, V2, V3, SVc, V4 (TO MARGIN DRIVE UNIT 700)
E
RD
WR
DD0~DD7
DS2
DSO
ADWR
623
625
621
605
611
603
601
613
619
641
630
645
643
650
671
673
675
661
690
667
663A
663B
663C
663D
665
669
677
680

FIG. 11

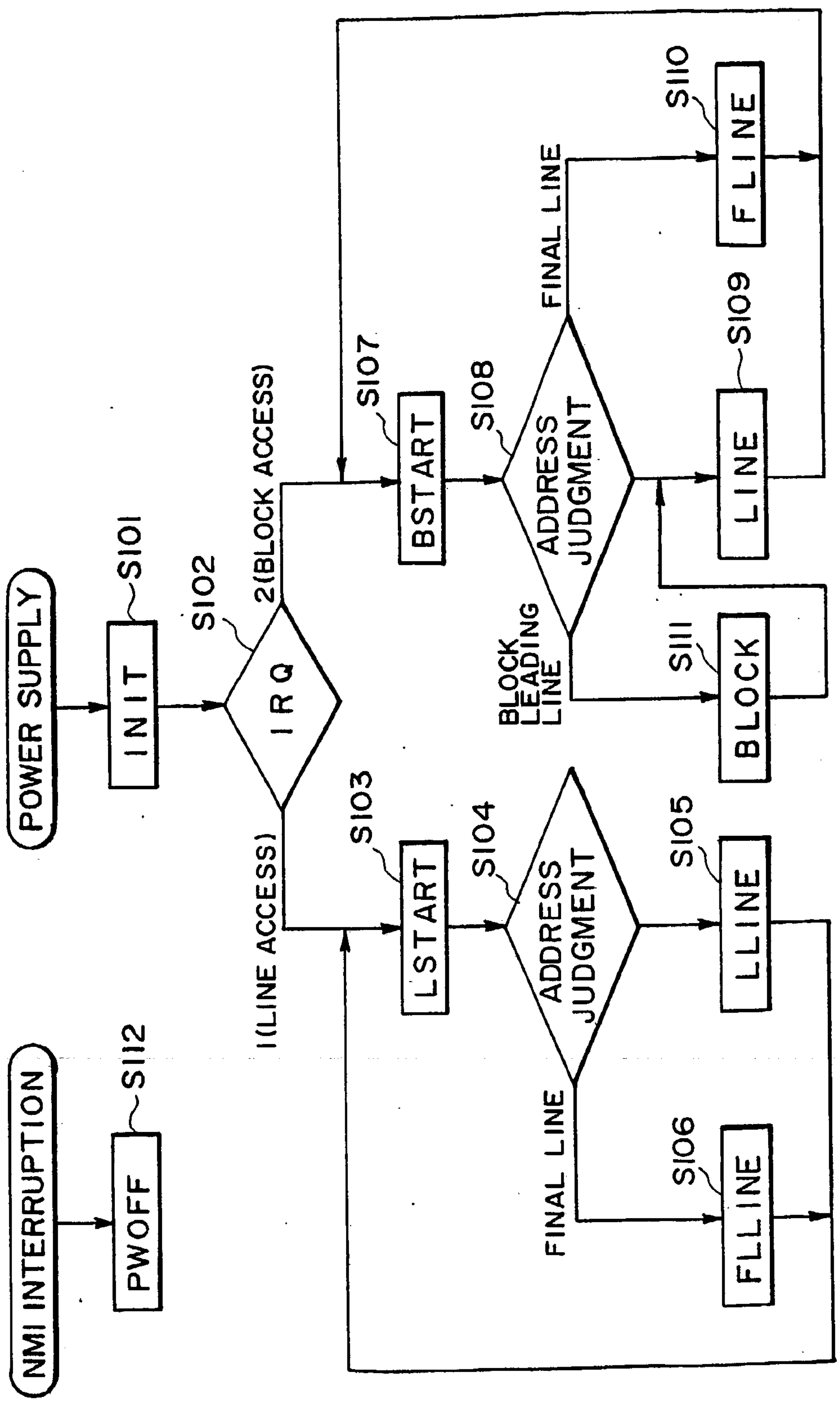
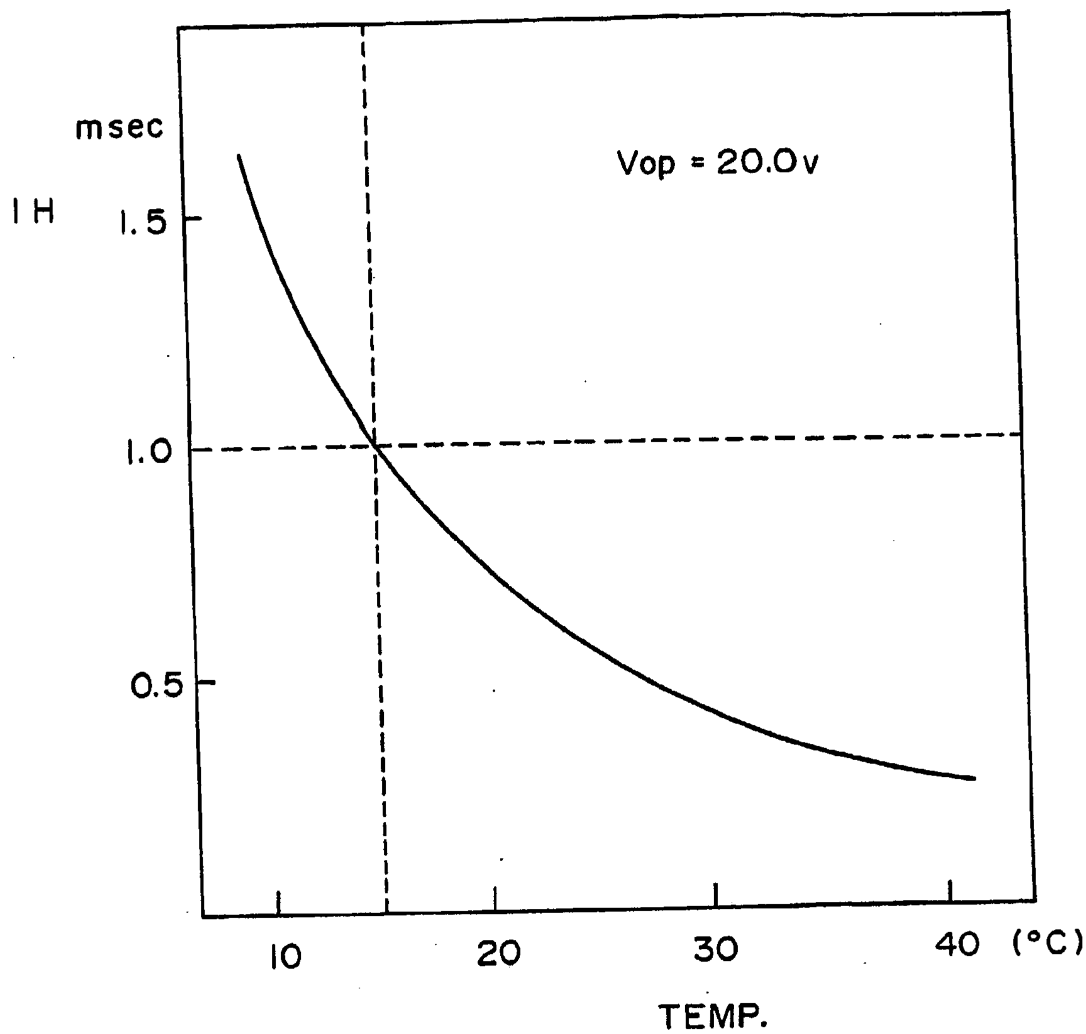
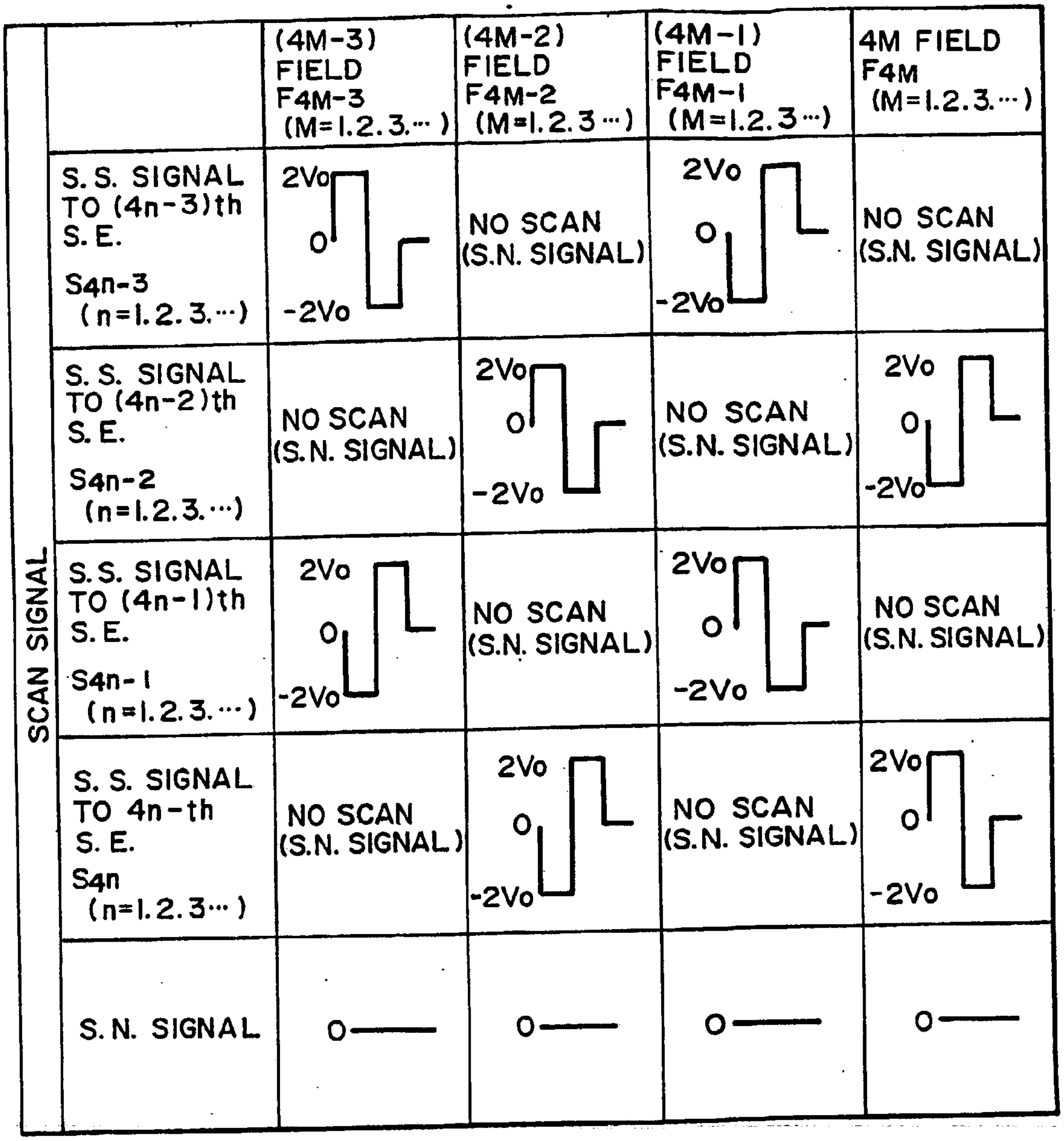

POWER SUPPLY
INIT
S101
IRQ
S102
1(LINE ACCESS)
2(BLOCK ACCESS)
LSTART
S103
ADDRESS JUDGMENT
S104
LLINE
S105
FINAL LINE
FLLINE
S106
BSTART
S107
ADDRESS JUDGMENT
S108
LINE
S109
FINAL LINE
FLINE
S110
BLOCK LEADING LINE
BLOCK
S111
NMI INTERRUPTION
PWOFF
S112

FIG. 12

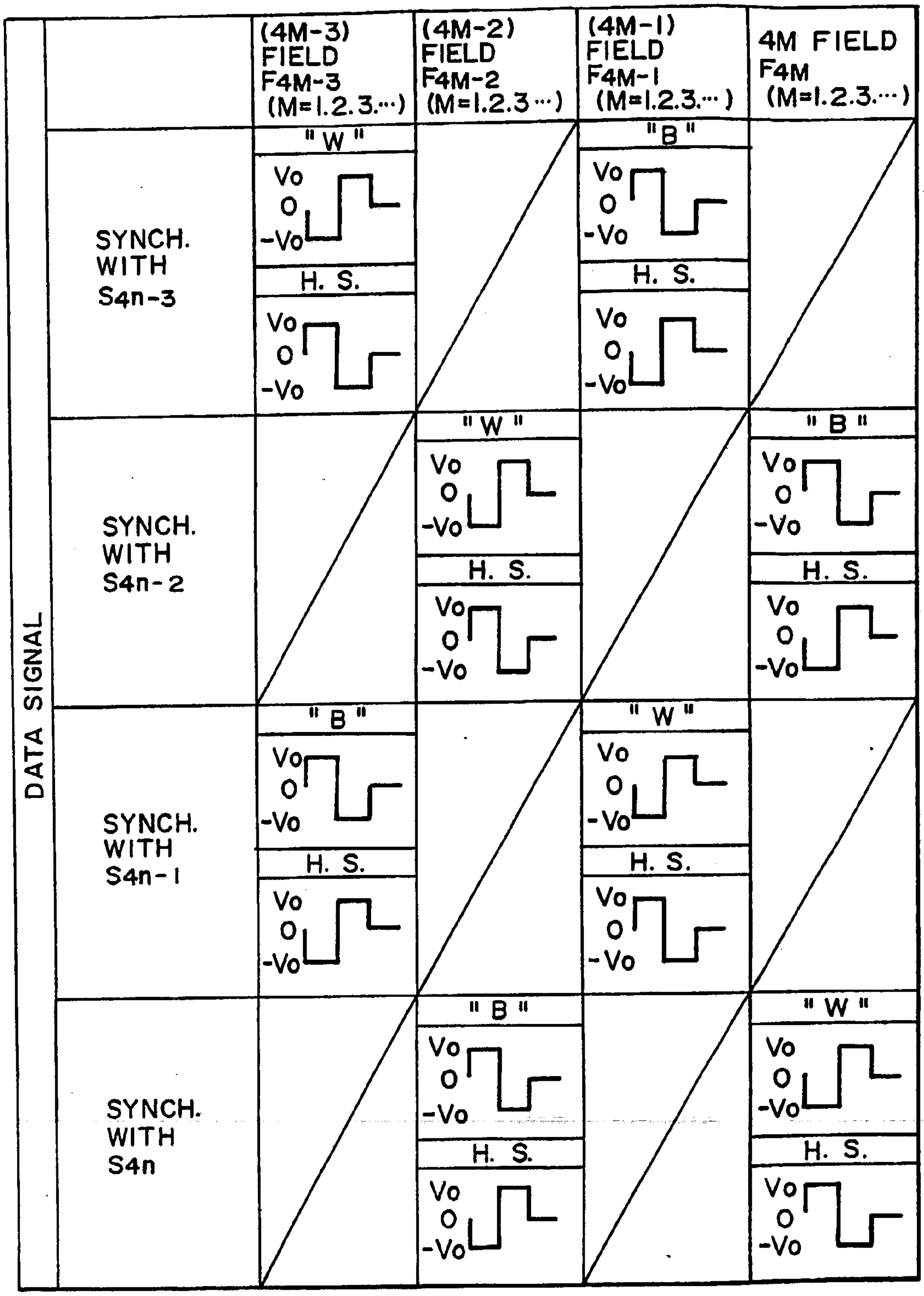


F I G. 13



S. S. = SCANNING SELECTION
S. N. = SCANNING NON-SELECTION
S. E. = SCANNING ELECTRODE

FIG. 14A



"W" = WHITE SIGNAL
"B" = BLACK SIGNAL
HS = HOLD SIGNAL

FIG. 14B

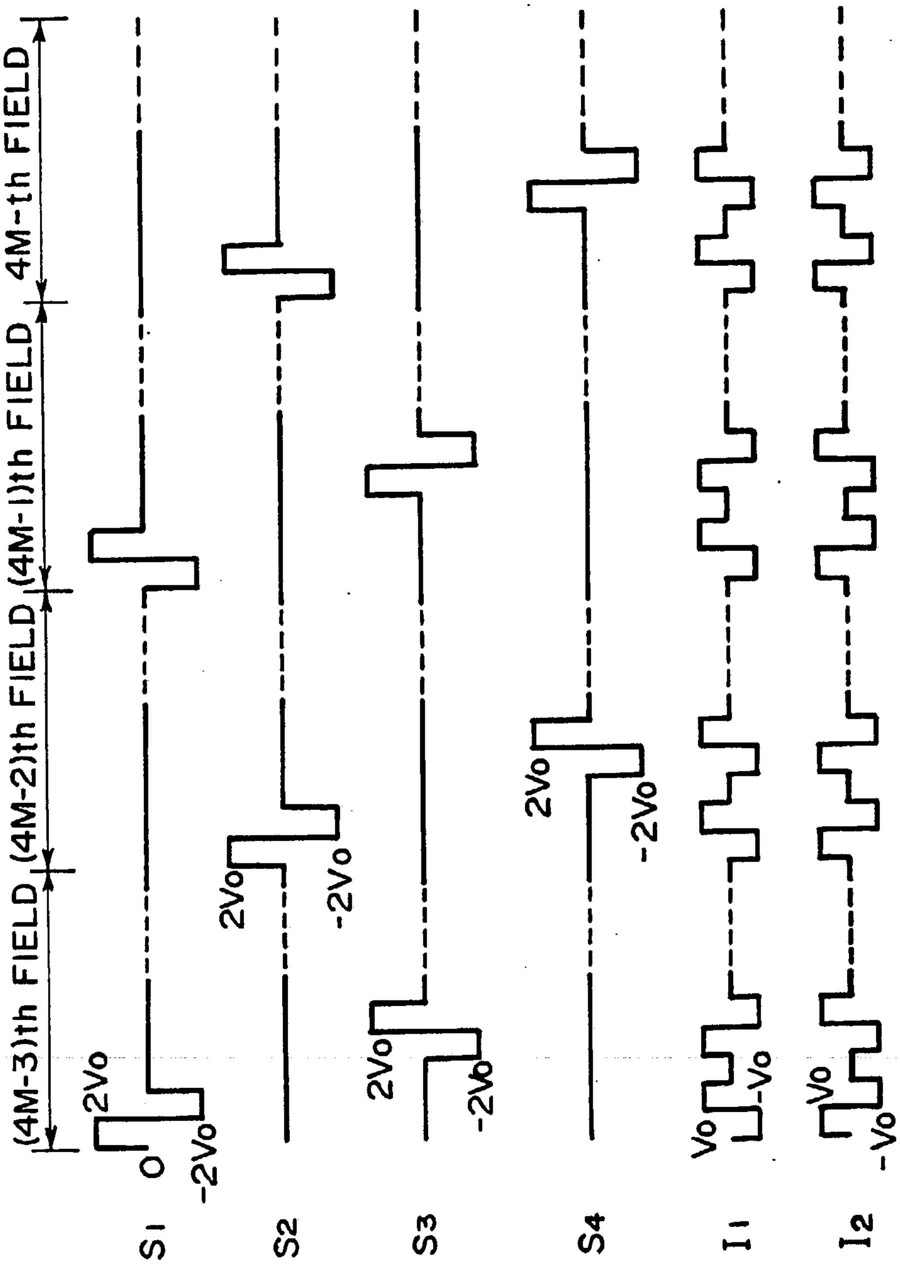

(4M-3)th FIELD
(4M-2)th FIELD
(4M-1)th FIELD
4M-th FIELD
S1
S2
S3
S4
I1
I2
2Vo
-2Vo
0
Vo
-Vo

FIG. 15A

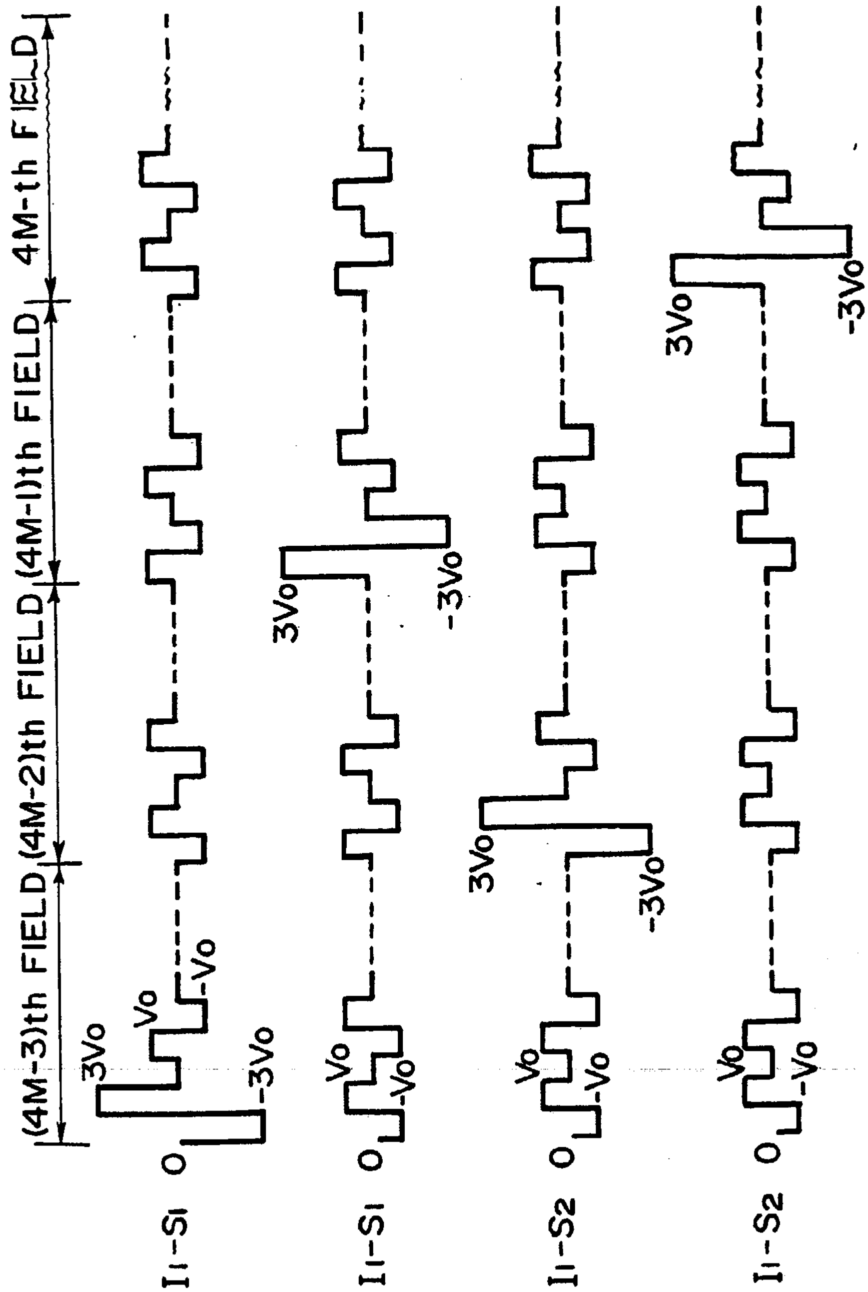

(4M-3)th FIELD
(4M-2)th FIELD
(4M-1)th FIELD
4M-th FIELD
3Vo
Vo
-Vo
-3Vo
O
I1-S1
I1-S1
I1-S2
I1-S2

FIG. 15B

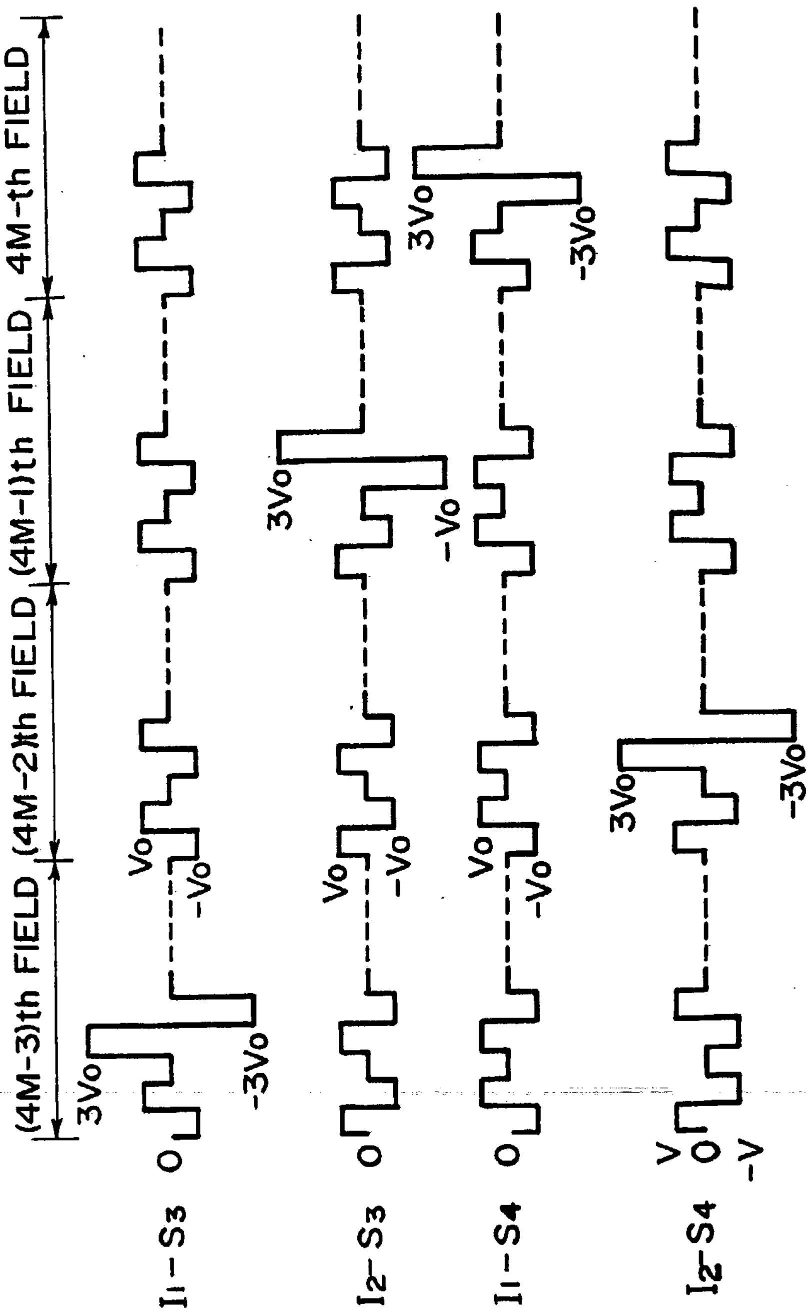
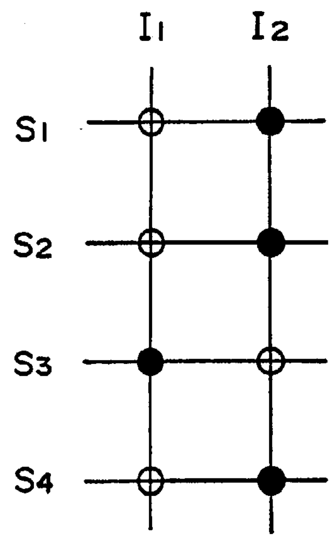

(4M-3)th FIELD
(4M-2)th FIELD
(4M-1)th FIELD
4M-th FIELD
I1-S3
I2-S3
I1-S4
I2-S4
3Vo
Vo
0
-Vo
-3Vo
V
-V

FIG. 15C



F I G. 15D

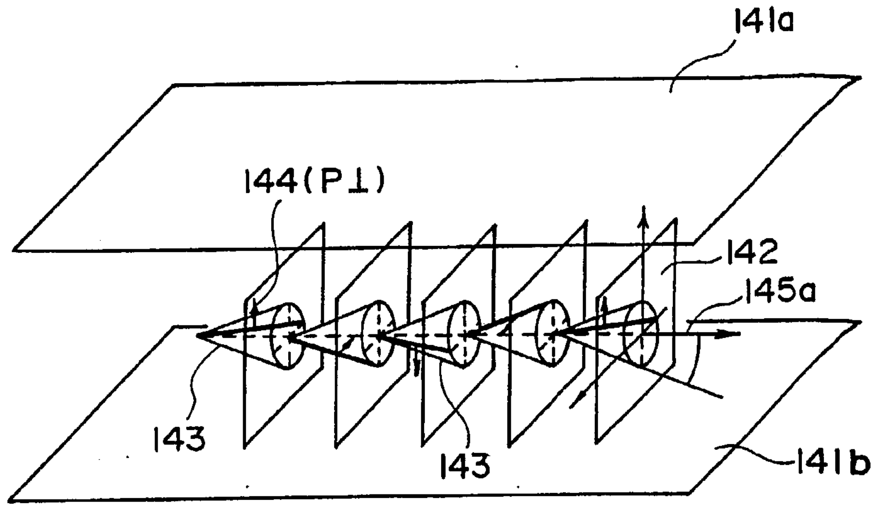

141a
144(P⊥)
142
145a
143
143
141b

FIG. 16

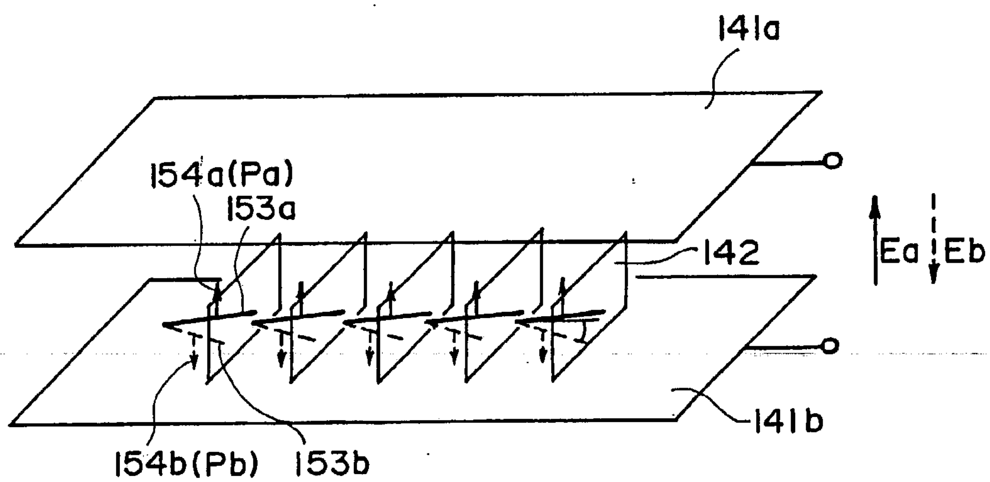

141a
154a(Pa)
153a
142
Ea
Eb
154b(Pb)
153b
141b

FIG. 17